CSE 452/552: VLSI Testing – Spring 2009

Lecture Hours: Mondays 5:00 pm – 7:40 pm (103 Talbert)
Instructor and E-mail address: Dr. Shambhu J. Upadhyaya, 129 Bell; shambhu@cse.buffalo.edu
Office Hours: Tuesdays 9:30 – 11:00 am
Teaching Assistant and E-mail address: XXX; xxx@cse.Buffalo.EDU
TA Office Hours: TBD.

Recommended Books:

- Lecture Notes, Available from the Web page (http://www.cse.buffalo.edu/faculty/shambhu/cse45209/).
- M. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers, 2000.
- N. Weste and K. Eshraghian, Principles of CMOS VLSI Design, Addison-Wesley, 1993.
- M. Abramovici, M.A. Breuer and A.D. Friedman, Digital Systems Testing and Testable Design, Computer Science Press, 1990.
- IEEE Design and Test of Computers Magazine.

Course Description, Objectives and Expectations:

Testing generally follows design, but often, they are interlinked. The objective of this course is to master the concepts of parametric and functional testing, test pattern generation, built-in testing of VLSI circuits, analog circuit testing and diagnosis. The following topics will be discussed in the class: VLSI Testing – Why and How? Test Generation, ATPG, Fault Model, CMOS Circuits, Design for Testability, Built-in Self-Testing, Partial Scan Techniques, Simulation at various levels – Switch level, Gate level and Behavioral level. Software Tools and Equipments for Testing, Advanced Concepts – Semi-custom VLSI Chips – Wafer-Scale-Integration, Multi-Chip Modules, System-on-Chip, Case studies – Microprocessor testing, Testing of RAMs. At the end of the course, the students are expected to be able to gain the skills to modify a given circuit and make it testable using the concepts and tools learned in the class.

Laboratory and Design Experience:

One project on module design using verilog/vhdl, one project on chip testing using tester from National Instruments, and one project on test synthesis using Cadence tools and several program-oriented exercises. You are expected to use the testable design guidelines learned in the class and incorporate them into your circuit at the design stage.

Grading Policy:

Homework and projects (40%), Two Midterms (30% each). The first midterm will be given on March 2nd and the second midterm will be given on April 27th. Both tests will be given in the class.

Academic Integrity:

The value of our courses, grades, degrees and research findings are dependent upon adherence to standards of ethical conduct. Plagiarism and inappropriate collaboration will not be tolerated. In this course we will adhere to the departmental standard for academic integrity. For more details, refer to the class webpage.