Name____

CSE 241 Digital Systems **Hourly Exam #2** April 3, 2009

Instructions: Write your name on the top of each sheet. Show all work in the space provided. No calculators or other electronic devices allowed. 50 min closed book.

1. Consider the Boolean function f(w,x,y,z) which is equal to 0 when its last variable z equals the binary sum of its other three variables, else f(w,x,y,z) equals 1.

(b) There are 6 size-4 subcubes and 1 size-1 as shown in answer box.

(c) Each one of the 7 subcubes above contains an essential 1-cell. So all 7 are irredundant and the minimal DNF is their sum.

(a) Draw the Karnaugh Map for f(w,x,y,z) showing the prime implicant subcubes.

		yz			
		00	01	11	10
wx	00	0	1	0	1
	01	1	0	1	1
	11	1	1	1	1
	10	1	0	1	1

(b) List all prime implicants

wz', xz', yz', wx, wy, xy, w'x'y'z

(c) Find a minimal DNF

wz'+ xz'+ yz+ wx+ wy+ xy+ w'x'y'z

2. $f(x,y,z) = (x+y)(x'+z')+xyz$

(a) Use the Quine-McCluskey Algorithm to find all the prime implicants of f. Show your work.

(b) Use the Petrick Method to find the set of all irredundant prime implicant DNF's. Show your work.

(a) $f = xx'+xz'+x'y+yz'+xyz = xz'+x'y+yz'+xyz$ so the truth table for f(x,y,z) is:

xyz	f
000	0
001	0
010	1
011	1
100	1
101	0
110	1
111	1

2(a)

010 √	01- √	-1-
011 √	1-0	
100 √	-10 √	
110 √	-11 √	
111 √	11- √	

So there are just two prime implicants: xz', y

So there are just two prime implicants: xz', y

2(b) Table of prime implicants:

	010	011	100	110	111
A 1-0			x	x	
B -1-	x	x		x	x

f= BBA(A+B)B=AB. So the unique irredundant DNF.is f=y+xz'

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3. (a) What is the main advantage of a carry look ahead adder over a ripple adder?

(b) What is the main advantage of a n-bit comparator built by cascading n 1-bit comparators over an n-bit comparator which is a minimal DNF realization?

(c) How many more gates does it take to build a 16-bit binary adder/subtracter than a 16-bit binary adder? Assume you can use only AND and OR gates.

3(a)

Speed. We don't have to wait for the carry bits to ripple forward.

3(b)

Just one type of module needed (1-bit comp). Note this is both slower and has more gates than a min DNF 16 bit comp circuit.

3(c)

One XOR gate per bit, or a total of 48 AND/OR gates for a 16 bit circuit.

4. **f(w,x,y,z) = w + w'x(y+z)'**

(a) Design a circuit which uses the given 16-to-1 MUX shown in Fig. 4(a) below to realize the Boolean function **f(w,x,y,z)**. Label all data and select input lines with their proper constant and literal values.

(b) Repeat using the 2-to-1 MUX shown in Fig. 4(b) below. Label all data and select input lines with their proper constant values, literal or Boolean expressions, and show all additional gates needed to realize f. Choose your select input variable (w, x, y or z) so that the <u>minimum number of additional gates</u> beyond the MUX iteself are needed.

f = w+w'x(y+z)' = w+w'xy'z'
So f=1 when w=1, ie. data inputs 1000 through 1111 (I_8 through I_{15}), and when w'xy'z'=1, data input 0100 or I_4. Otherwise f=0.

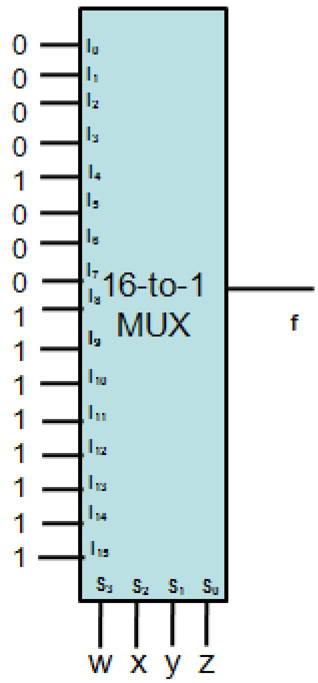

Figure 4a

If we use w as the select input, then when w=0 f_0=0+1xy'z'=xy'z' and when w=1 f_1=1+0xy'z'=1 so only one AND gate needed. If use x, f_0=w+w'0y'z'=w and f_1=w+w'y'z' so we need one AND and one OR. Same if use y or z as the select input. So choose w in which case inputs are f_0=xy'z' and f_1=1.

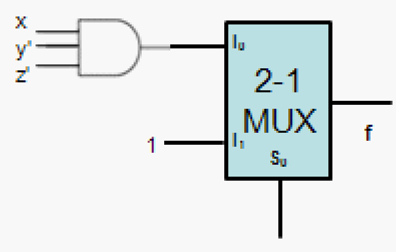

Figure 4b

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