Title:
An Integrated Framework for Test Scheduling and Control in Complex SoCs

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Abstract:

System-on-a-chip (SoC) is evolving as a new design style, where an entire system, integrating analog, digital, and memory circuit, is built on a single chip. Reusing IP (intellectual property) cores can shorten time-to-market of a new system while meeting various design requirements such as high performance, low power and low cost. However, without effective design-for-testability and test generation techniques, the SoC manufacturing test may become the bottleneck of the entire design process.

Since the IP cores are not manufactured and tested before integration into the system chip, the system integrators need to test not only the interconnects between the cores and user-defined-logics around the cores, but also the individual cores embedded in the system. With several hundreds of embedded components in a single package, test scheduling is necessary to run intra-core and inter-core tests, which reduces the test cost by a certain level of parallelism while meeting the test quality. In addition, a low-cost, efficient control network is needed to initialize test resources during test application and observe corresponding test results at appropriate instants.

In this proposal, we address two research issues: integrated design and optimization of SoC test solutions (specifically, the test scheduling algorithm design), and test control network design. We first present a general test model of SoCs for testability analysis, test scheduling and diagnosis. We then present different test scheduling algorithms for various SoC design styles and test environment, which reflects various test constraints such as resource sharing, power dissipation, and fault coverage, and develop an integrated framework combining wrapper design, test access mechanism (TAM) configuration and test scheduling. More specifically, we propose a fault model oriented test set selection scheme and formulate the test scheduling as a shortest path problem with the feature of evenly balanced resource usage. We further propose a dynamic test partitioning technique based on test compatibility graph to address the power-constrained test scheduling problem. Furthermore, we present an integrated framework to handle constrained scheduling in a way that constructs core access paths and distributes TAM bandwidth among cores, and consequently configures the wrapper scan chains for TAM width adaptation.

Using the "radio-on-chip" technology, we propose a new distributed multihop wireless test control network consisting of three basic components, the test scheduler, the local test control logic (TCL), and the clusterhead which supports the communication between the test scheduler and TCLs. Under the multilevel tree structure, several system optimization issues such as placement, cluster number and routing problems need to be addressed. Techniques are presented for the integration of test resource distribution (including not only the circuit blocks to perform testing, but also the on-chip radio-frequency
nodes for intra-chip communication) and system optimization among TAM design, test scheduling (concurrent core testing as well as interconnect testing) under power and cost constraints. Simulations using randomly generated test sets and experiments with benchmarks will be performed for evaluation and verification of the proposed test optimization algorithms.