LAST NAME: FIRST NAME: RECITATION: A1: Th 4-4.50pm☐
PERSON # : A2: Wed 1-1.50pm☐
CSE341 – COMPUTER ORGANIZATION – SPRING 2018 **Homework 10** A4: Th 3-3.50pm☐
Due: Friday May 11, 2018 10:00am (Mark your recitation on the right) A5: Wed 8-8.50am☐

1. In this exercise, we will look at the different ways capacity affects overall performance. In general, cache access time is proportional to capacity. Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows data for L1 caches attached to each of two processors, P1 and P2.

	L1 Size	L1 Miss Rate	L1 Hit Time
P1	2 KiB	8.0%	0.66 ns
P2	4 KiB	6.0%	0.90 ns

   a. Assuming that the L1 hit time determines the cycle times for P1 and P2, what are their respective clock rates?

   b. What is the Average Memory Access Time for P1 and P2?

   c. Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 and P2? Which processor is faster?

2. Consider a 2-level mixed cache with a level-0 hit rate of 96% and a level-1 hit rate of 78%. Calculate the local hit and miss rates for each level, followed by the global hit and miss rates for the entire cache.

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3. (Optional – for extra point 10 pts)

This exercise examines the impact of different cache designs, specifically comparing associative caches to the direct-mapped caches. For these exercises, refer to the address stream below.

3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253

a. Using the sequence of references above, show the final cache contents for a three-way set associative cache with two-word blocks and a total size of 24 words. Use LRU replacement. For each reference identify the index bits, the tag bits, the block off set bits, and if it is a hit or a miss.

b. Using the references above, show the final cache contents for a fully associative cache with one-word block and a total size of 8 words. Use LRU replacement. For each reference identify the index bits, the tag bits, and if it is a hit or a miss.