CSE341 - COMPUTER ORGANIZATION - SPRING 2018 HOMEWORK 6
(Show the steps) Due: Monday, April 2, 2018 10am

1. Examine the effect of pipelining on the clock cycle time of the processor. Assume the individual stages of the datapath have the latencies as given in Table 1. And the instructions executed by the processor are broken down as given in Table 2.

Table 1:

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

Table 2:

alu	beq	lw	sw
45%	20%	20%	15%

a. What is the clock cycle time in a pipelined and non-pipelined processor?

b. What is the total latency on a SW instruction in a pipelined and non-pipelined processor?

2. For a given processor, assume there are no stalls. The breakdown of executed instructions are as given in Table below:

add	addi	not	beq	lw	sw
20%	20%	0%	25%	25%	10%

a. In what fraction of all cycles is the data memory used? Why?

b. In what fraction of all cycles is the input of the sign-extend circuit needed? Why? What is this circuit doing in cycles in which its input is not needed?

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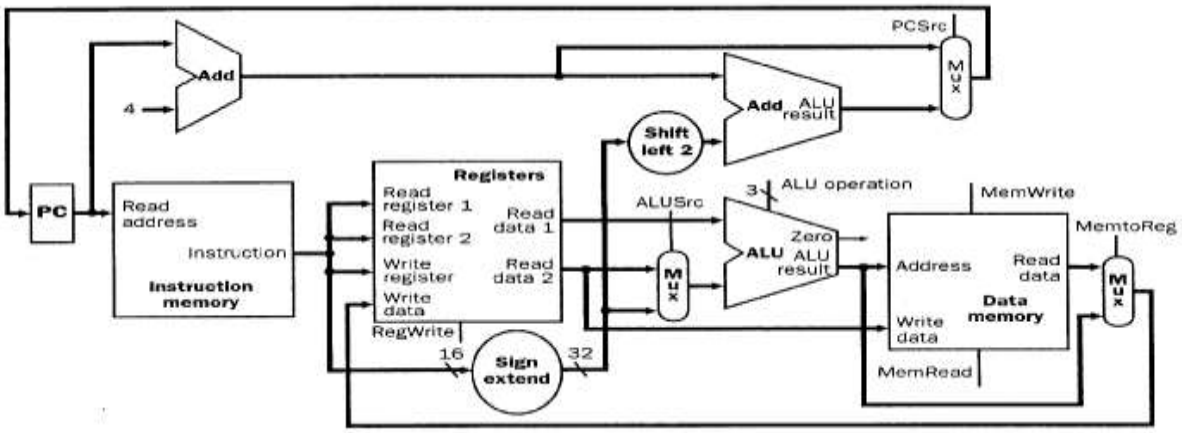
3. Highlight and explain the flow of data in the MIPS data path for
(a) ADD instruction and



(b) lw instruction