LAST NAME: FIRST NAME: RECITATION: A1: Th 4-4.50pm☐

PERSON # : A2: Wed 1-1.50pm☐

CSE341 – COMPUTER ORGANIZATION – SPRING 2018 **Homework 8** A4: Th 3-3.50pm☐

Due: April 16, 2018 10:00am (Mark your recitation on the right side) A5: Wed 8-8.50am☐

1. The processor fetches the following instruction word: 10101100011000100000000000010100.
   Assume that data memory is all zeros and that the processor's registers have the following values at the beginning of the cycle in which the above instruction word is fetched:

r0	r1	r2	r3	r4	r5	r6	r8	r12	r31
0	–1	2	–3	–4	10	6	8	2	–16

   a. What are the outputs of the sign-extend and the jump "Shift left 2" unit (near the top of Figure 1) for this instruction word?
   b. What are the values of the ALU control unit's inputs for this instruction?
   c. What is the new PC address after this instruction is executed? Highlight the path through which this value is determined.
   d. For each Mux, show the values of its data output during the execution of this instruction and these register values.
   e. For the ALU and the two add units, what are their data input values?
   f. What are the values of all inputs for the "Registers" unit?

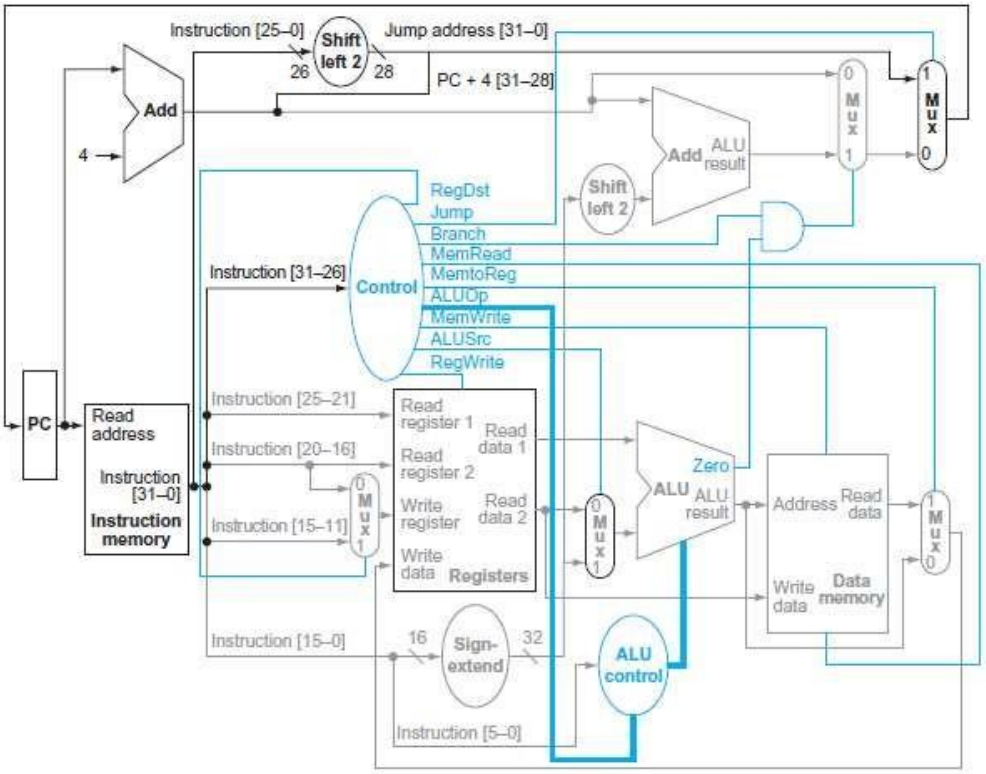

Figure 1. Simple control and datapath

2. Consider the following set of instructions:

   and $s4, $s5, $s6
   beq $s1, $s2, loop
   lw $s3, 0($s0)
   loop: add $s7, $v1, $v2

   Draw the 5-stage MIPS pipeline for the following initial register conditions:

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a.

$s0	$s1	$s2	$s3	$s4	$s5	$s6	$s7	$v1	$v2
1	4	4	2	3	2	3	6	5	4

b.

$s0	$s1	$s2	$s3	$s4	$s5	$s6	$s7	$v1	$v2
1	4	3	3	2	2	3	8	5	4

3. Consider the memory location 0x10000000 has the value 00000014.
$a3 holds the address 0x10000000 and $t1 holds the value 5.
Consider the following MIPS code sequence with a 5-stage pipeline without data forwarding:

```
addi $t1, $t1, 2
lw $t1, 0($a3)
addi $t2, $t1, 5
addi $t1, $t1, 12
```

What are the contents of the registers $t1, $t2 and $a3 after the code sequence above is executed?

4. Consider initial values of registers

$t1	$t2	$t3
1	7	5

Given below is a sequence of MIPS instructions with a 5-stage pipeline without data forwarding:

```
Loop: sll $t2, $t2, 1
      addi $t2, $t2, 1
      bne $t1, $t3, Loop
      addi $t1, $t1, 1
```

What are the contents of the registers $t1, $t2 and $t3 after the code sequence is executed?