LAST NAME: FIRST NAME: RECITATION: A1: Th 4-4.50pm☐

PERSON # : A2: Wed 1-1.50pm☐

**CSE341 – COMPUTER ORGANIZATION – SPRING 2018 Homework 9** A4: Th 3-3.50pm☐

Due: Friday May 4, 2018 10:00am (Mark your recitation on the right) A5: Wed 8-8.50am☐

1. Below is a list of 32-bit memory address references, given as word addresses.
   3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253

a. For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

b. Given Cache Data Size 32 Kilo Bytes and Cache Block Size is 2 words. Calculate the total number of bits required, assuming a 32-bit address. Given that total size, find the total size of the closest direct-mapped cache with 16-word blocks of equal size or greater. Explain why the second cache, despite its larger data size, might provide slower performance than the first cache.

2. For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

| Tag | Index | Offset |
|---|---|---|
| 31–10 | 9–5 | 4–0 |

Starting from power on, the following byte-addressed cache references are recorded.

| Address | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 4 | 16 | 132 | 232 | 160 | 1024 | 30 | 140 | 3100 | 180 | 2180 |

a. What is the cache block size (in words)?

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b. How many entries does the cache have?

c. How many blocks are replaced?

d. What is the hit ratio?

e. List the final state of the cache, with each valid entry represented as a record of <index, tag, data>.