CSE 493/593 Test 1 Solution Fall 2011 **Total Points: 100**

1. Short question

(a). Why do we gradually increase the size of inverters in buffer design? Why not give the output of a circuit to one large inverter? (6)

Ans:

Minimize total propagation delay.

(b). What is skin effect? When is it more of a challenge-at low or high frequencies? (6)

Ans:

Skin effect is all of the current flows on the outside portion of a wire. It occurs more at higher frequencies.

(c). Consider the static CMOS gate shown in Fig.1. Assume V_{dd} = 2.5V and V_{Tn} = 0.5V. Will the threshold voltages of the two NMOS transistors be the same? If yes, why? If not, why not? (6)

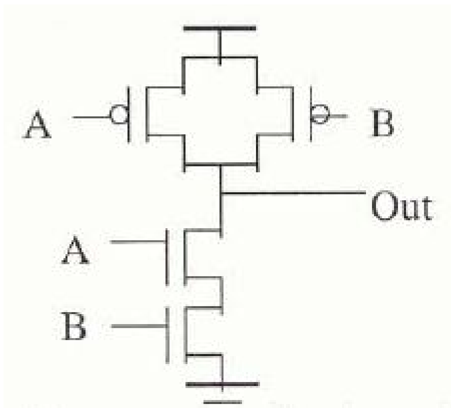


Fig.1

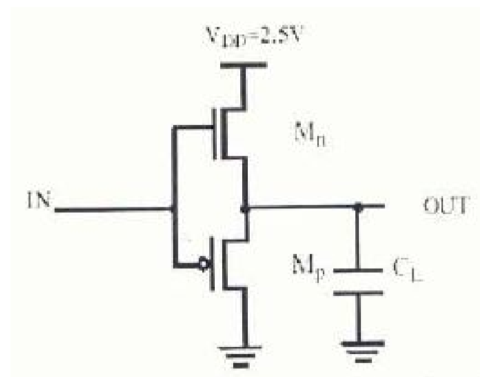


Fig.2

Ans:

No, the threshold voltages are not the same, due to body effect on the first NMOS in the PDN.

(d) For each of the following, indicate whether it is True of False. (6)

(i) Long wires have low resistance.

Ans:

False. $R = \frac{\rho l}{wh}$, so long wires have high resistance.

(ii) Wide wires have high resistance.

Ans:

False. $R = \frac{\rho l}{wh}$, so wide wires have low resistance.

(iii) The load capacitance of a static CMOS gate has no effect on its VTC.

Ans:

True. VTC does not depend on load capacitance.

2. Consider an unconventional buffer/driver circuit (similar to an inverter circuit) as shown in Fig.2, where the pull-up is an NMOS device and the pull-down is a PMOS device. Ignore body effect and channel-length modulation. (10)

(a) What should the bulk terminals of the NMOS and PMOS be connected to, respectively and why?
Ans: (5 points)
Bulk of NMOS: Gnd
Bulk of PMOS: Vdd
Reason:

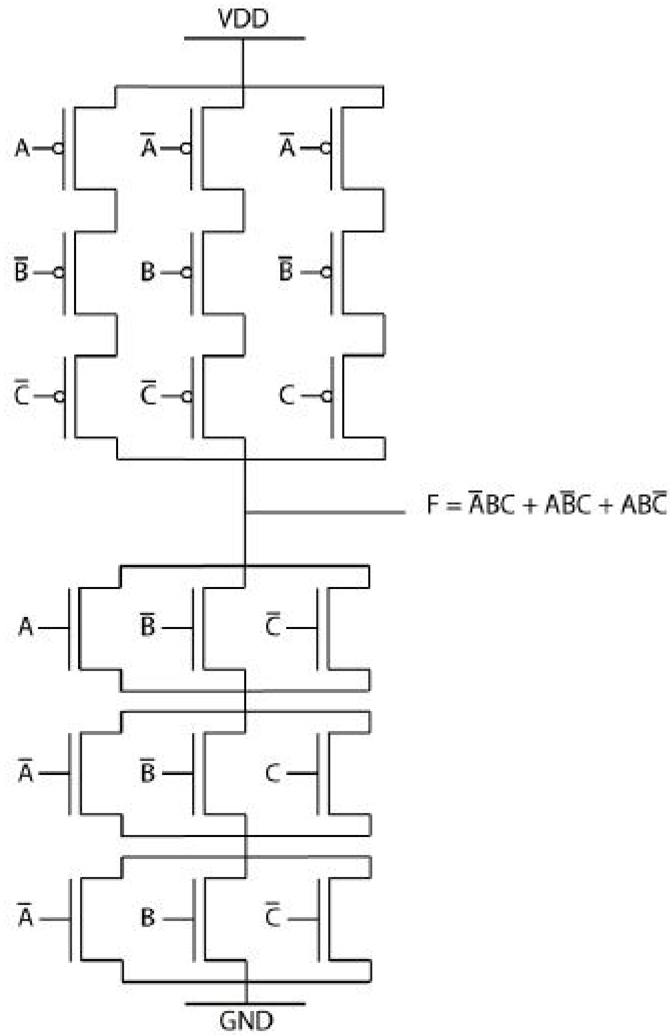
In MOS transistors, the pn junction diodes of source-bulk and drain-bulk are a big thread for the performance and power consumption of devices. Therefore, to turn off these diodes, the bulk or substrate of NMOS must always be connected to the lowest voltage that is the Gnd and the bulk of a PMOS must always be connected to the power supply voltage.

(a) *n*MOS transistor (b) *p*MOS transistor

(b) What the values of V_{out} when V_{in} = 0 and $V_{in} = V_{dd}$. Explain. Assume V_{dd} = 2.5V
Ans: (5 points)
Vin=0, Vout=|Vtp|
Vin=Vdd, Vout=Vdd-Vtn

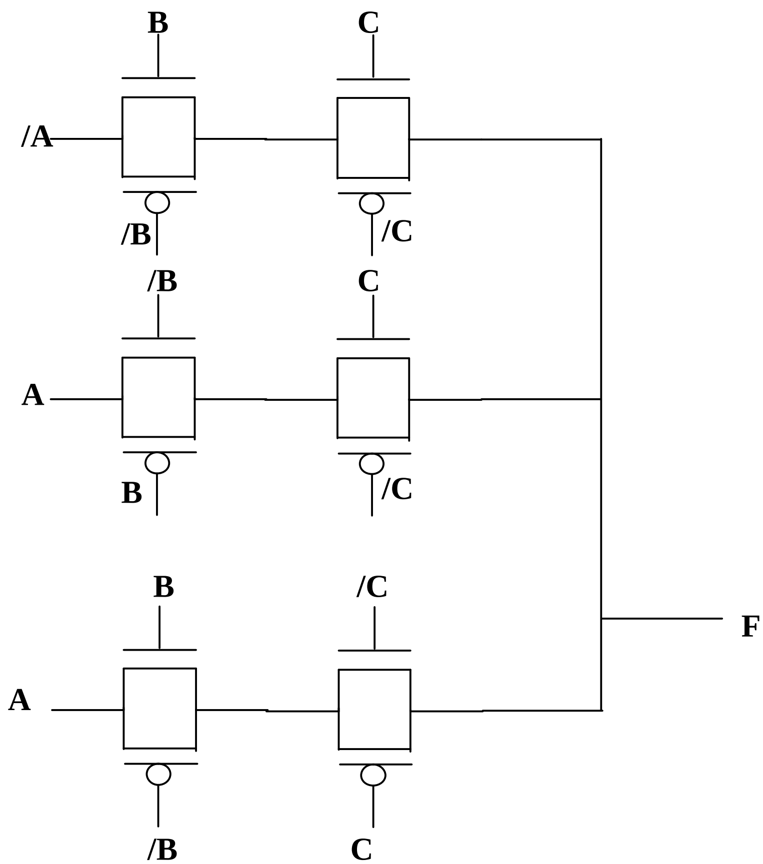
3. Consider the function Y = A'BC + AB'C + ABC' (10)
(a). Implement the above expression in compound CMOS logic style (PUN and PDN). (3)
Ans: On Next page.

(b). Which input pattern(s) would give the worst and best case equivalent pull-up and pull-down resistance?
Ans: (4)
Pull Up Network: Best & Worst delay: 011, 101, 110
Pull Down Network: Best delay:000 Worst Delay: 111


VDD
A
Ā
Ā
B̄
B
B̄
C̄
C̄
C
F = ĀBC + AB̄C + ABC̄
A
B̄
C̄
Ā
B̄
C
Ā
B
C̄
GND

(c). Implement the above expression in Transmission logic style. (3)

Ans:



4. (**a**) Determine the region of operation and the drain current I_D for the PMOS transistor with k_p' =30uA/V^2, V_{T0}=-0.8V, λ=0.1V^{-1}, (W/L)=1, V_{GS} = -0.5V, V_{DS}=-1.5V. (6)

Ans:

V_{GS} = -0.5V, V_{T0}=-0.8V, V_{GS}>V_{T0}, so PMOS is cut-off. I_D=0.

(**b**) The VTC of an inverter is shown in Fig.3. Using the plot, compute the V_{OH}, V_{OL}, V_{IH}, V_{IL}, N_{ML} and N_{MH} values of the inverter. Show your work. (10)

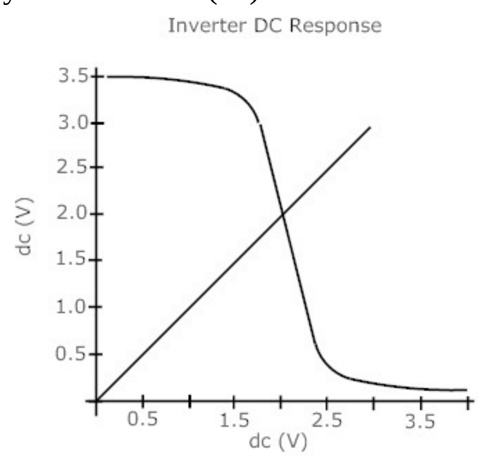


Fig.3

Ans:

For the linear region, Find V_{OH}, V_{OL}, gain and V_M from the graph: V_{OH}= 3.5V, V_{OL}=0.2V, g=-5, V_M=2V

$V_{IH}=V_M-V_M/g=2-2/(-5)=2.4V$

$V_{IH}-V_{IL}=-(V_{OH}-V_{OL})/g$

So $V_{IL}=V_{IH}+(V_{OH}-V_{OL})/g=2.4-3.3/5=1.74V$ e that the capacitor is initially discharged and **ignore subthreshold** conduction and body effects. (

$N_{ML}=V_{IL}-V_{OL}=1.74V$, $N_{MH}=V_{OH}-V_{IH}=0.9V$

5. Find the final value of the voltage V_o in each case. Assume $V_{Tn} = |V_{Tp}| = 0.5V$. Assum12)

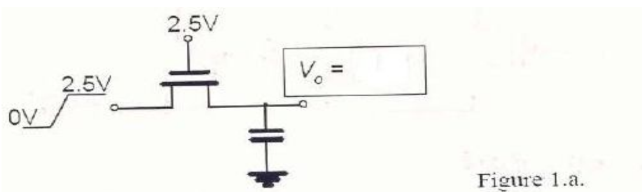


Figure 1.a.

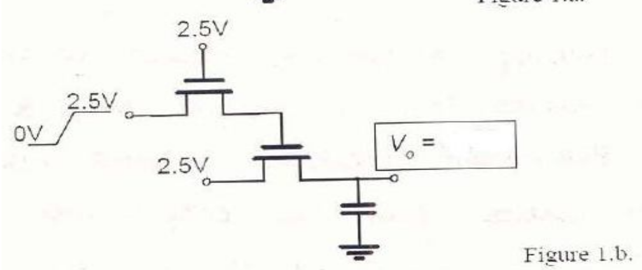


Figure 1.b.

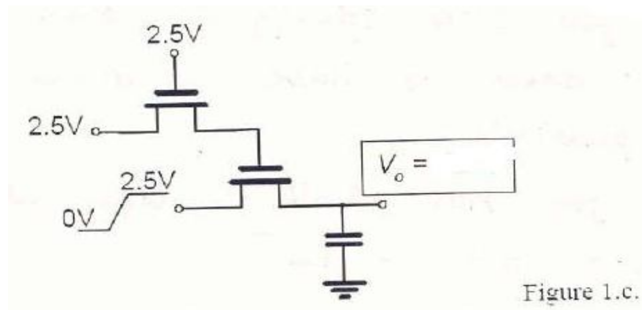


Figure 1.c.

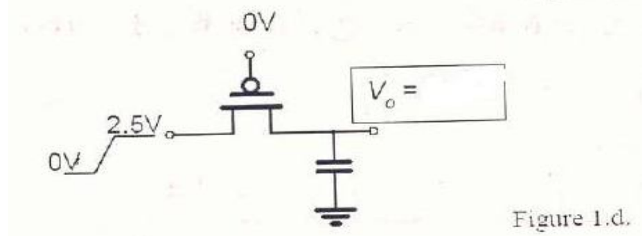


Figure 1.d.

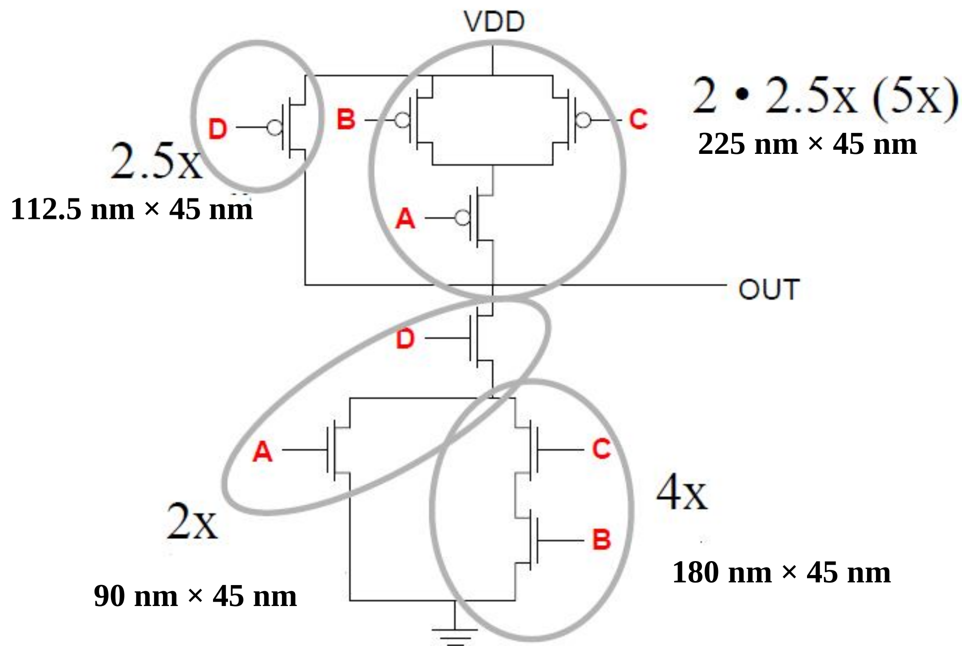
Ans: (3 points each)

(a) 2 V
(b) 1.5 V
(c) 1.5 V
(d) 2.5 V

6. Consider the function $out = \overline{(a + b \cdot c) \cdot d}$. Draw the circuit and size the transistors: size all NMOS and PMOS transistors so that the PUN and PDN each has equivalent resistance to a minimum-sized NMOS, and then take into account the fact that µn= r • µp where r = 2.5 (i.e. the resistance of a unit PMOS device is 2.5 times that of a unit NMOS device). (12)

Note: Assume the circuit is im plemented in a 45nm technology and that the dimensions of a minimum-sized MOSFET in this technology are 45nm width x 45nm length. Express the dimensions of each MOSFET in the optimized circuit in nanometers (W nm x L nm).

Ans: Schematic- 4 points; sizing – 4 points; specific value of each transistor – 4 points.



7.
(a). In order to drive a large capacitance (C_L = 20 pF) from a minimum size gate (with input capacitance C_i = 10fF), you decide to introduce a three-staged buffer. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the three additional buffer stages that will minimize the propagation delay. (8)
(b). If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case? (8)

Ans:
(a) In this problem, the number of stages N = 4, $C_L = 20pF$, $Ci = 10fF$.

$$f = \sqrt[N]{\frac{C_L}{C_{in}}} = \sqrt[4]{\frac{20\,pF}{10\,fF}} = 6.7$$

Minimum delay occurs when the delay through each buffer is the same. This can be achieved by sizing the buffers as 6.7(W/L), 6.7^2(W/L) , 6.7^3(W/L)respectively

(b)

To achieve minimum delay, Let $f = \sqrt[N]{\frac{C_L}{C_{in}}} = \sqrt[N]{\frac{20\,pF}{10\,fF}} = e$

So we can obtain N=7.6 .
We choose N=7
When N=7,
$t_p = Nt_{p0}(1 + f/\lambda)$ =1.9ns