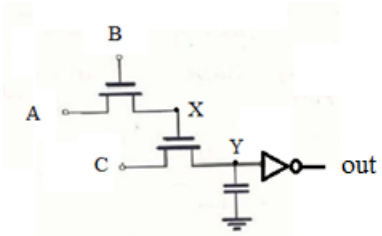
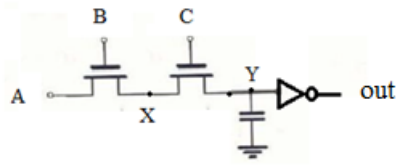
CSE 493/593 Homework 2 Fall 2023

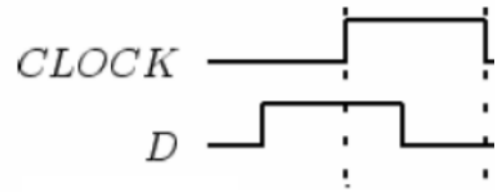
1. Design a Half adder using CPL technology.
   Considering A and B are the inputs, Sum and Carry are the outputs
2. Determine the logic function implemented by
   i.



   ii.



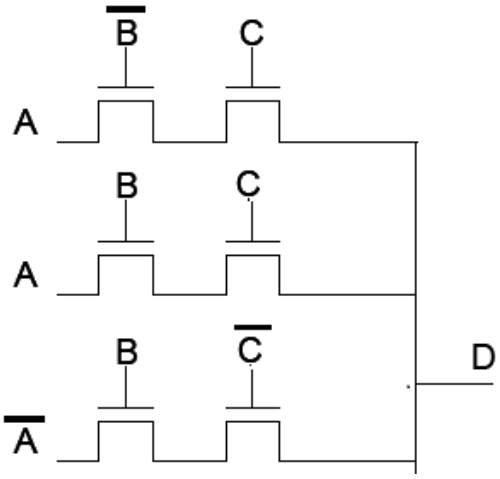
3. Answer the following:
   i. What's difference in the function between a D latch and a D flip-flop?
   ii. Complete the timing diagrams for a positive-level-sensitive D latch and a positive-edge-triggered D flip-flop



Latch Q

Flipflop Q

4. Consider the circuit in Fig. below. What is the logic function implemented by this Circuit?



5. How can you manipulate threshold voltage using body-biasing?

6. The figure shows the input and output signals of a CMOS inverter. Calculate the following using the time instances mentioned in the figure.
    a. Fall time
    b. Rise time
    c. Propagation delay