# CSE 493/593 FALL 2023

## HOMEWORK 3

1. In order to drive a large capacitance (CL = 20 pF) from a minimum size gate (with input capacitance Ci =10fF), you decide to introduce a three-staged buffer. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size.

   (Hint: Sizing factor $f = \sqrt[N]{C_L / C_{g,1}} = \sqrt[N]{F}$ ;

   Minimum delay through the chain $t_p = Nt_{p0}(1 + \sqrt[N]{F}/\gamma)$

   a. Determine the sizing of the three additional buffer stages that will minimize the propagation delay.

   b. If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case? Consider γ=1.

2. Implement the given logic function using Complementary CMOS logic. (Transistor level diagram). F = ^[((A+B)C+D)EF]

   Size all the transistors for
   a. Performance
   b. Symmetric rise and fall times