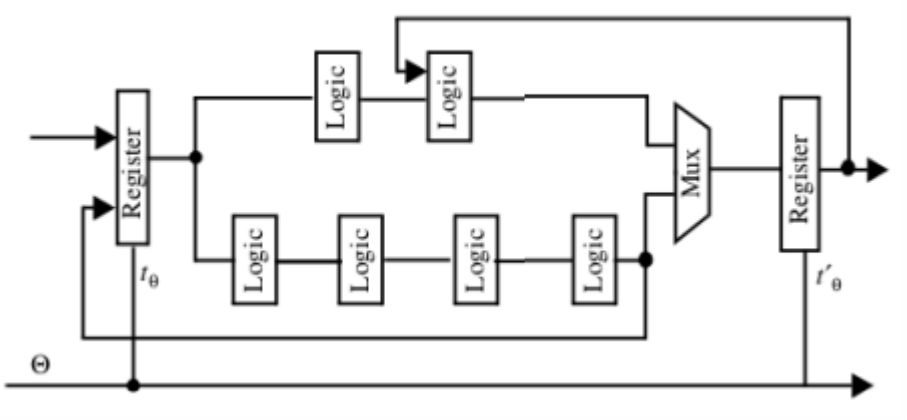
CSE 493/593 FALL 2023 HOMEWORK 5

1. Explain Clock skew and clock jitter.

2.
   a. Explain how Dynamic Frequency Scaling can achieve low power.
   b. Explain how Dynamic Voltage Scaling can achieve low power.

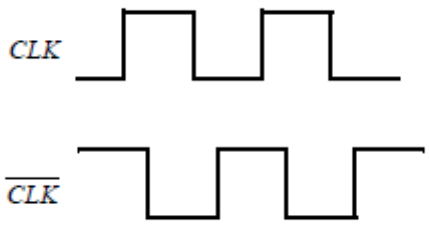
3. For the circuit shown below, assume a unit delay through the register, multiplexer and logic blocks. Assume that the registers, which are positive-edge triggered, have a unit setup time.



   Determine minimum clock period disregarding clock skew.
   (Hint: T ≥ tc-q + tlogic + tsu)

4. Describe how H-tree clock distribution scheme achieves the following:
   a. Reduced clock skew
   b. Reduced power consumption

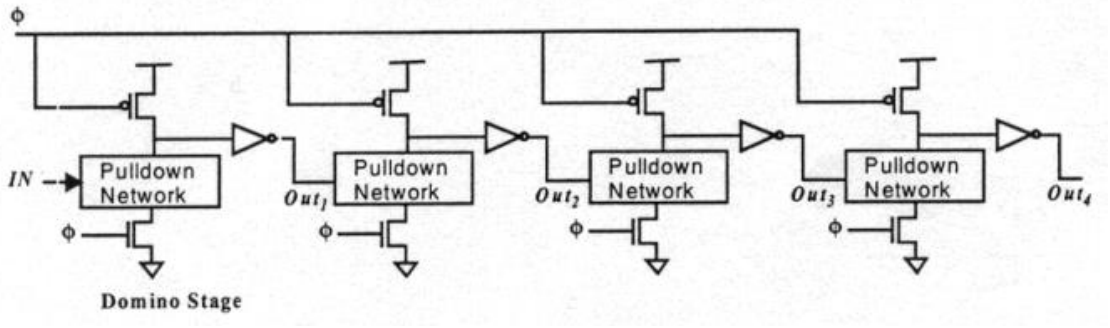
5. From the clock waveform given below,

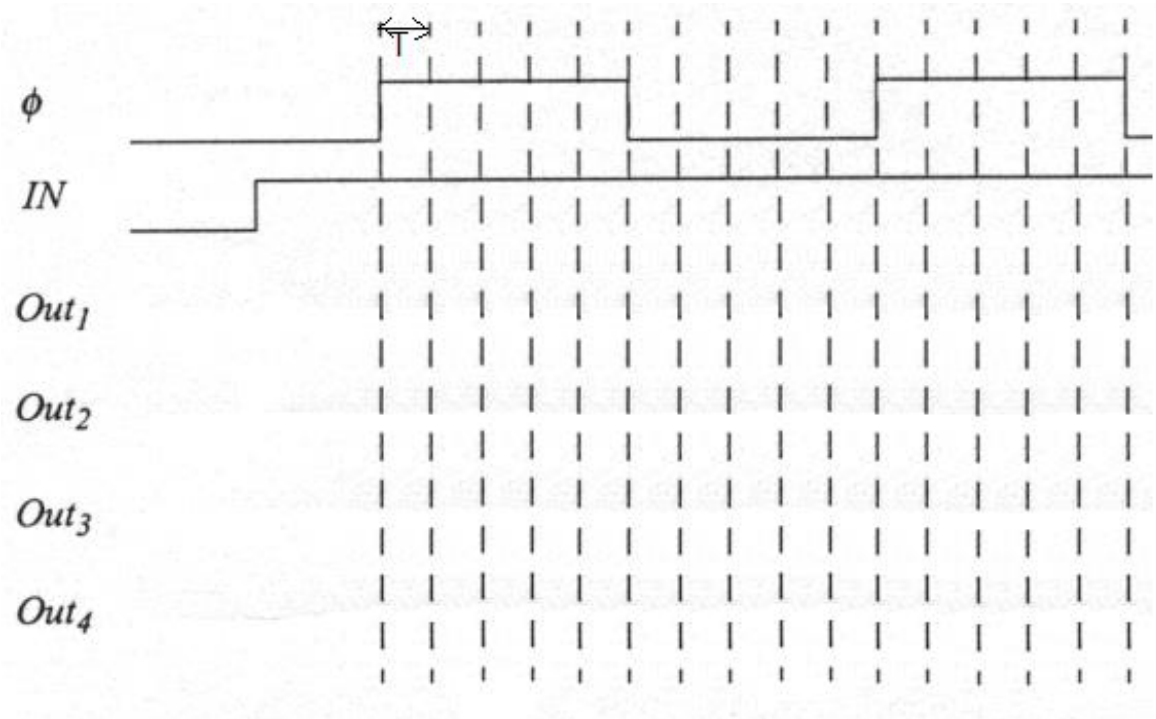


   a. identify regions of (1,1) overlap and (0,0) overlap.
   b. How can you overcome this issue?
   (Hint: From the truth table of a Full Adder, derive the SUM and CARRY equations and then design the logic)

6. Consider the logic function X = ^((A(B+CD)E)+(FG(H+I))). Implement the function using Dynamic CMOS Logic.

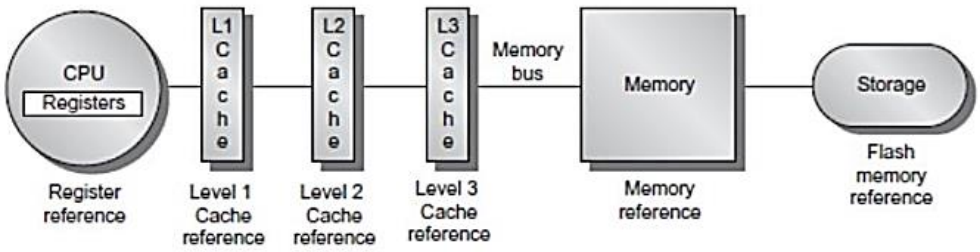
7. Consider the 4-stage domino logic circuit as shown below. Assume that each of the PDN in the figure has a single NMOS transistor. Assume the precharge time, evaluate time, propagation delay of the static inverter are all equal to T/2 each (with T a time unit). Also assume zero rise and fall times for all signals. Complete the timing diagram for signals Out1, Out2, Out3 and Out4 if the IN signal goes high at the rising edge of the clock ϕ. Assume clock period is T.





8. Implement SUM and CARRY of a Full Adder in DCVSL. Assume A, B, C and their complements are available as inputs

9. Given a typical memory hierarchy as shown below, list them in increasing order of
   a. Speed
   b. Cost per unit memory
   c. Size



10. Draw the schematic of 6T SRAM and explain how it's working.