A New Distributed Test Control Architecture with Multihop Wireless Test Connectivity and Communication for GigaHertz System-Chips (Extended Summary) [*]

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Abstract

With the increase in chip size and complexity, the direct or bus interconnects in conventional SoC test control models are rather restricted. In this paper, we propose a new distributed multihop wireless test control network based on the recent development in "radio-on-chip" technology. The proposed architecture consists of three basic components, the test scheduler, the resource configurators, and the RF nodes which support the communication between the test scheduler and clusters of cores. Under the multilevel tree structure, the resources (including not only the circuit blocks to perform testing, but also the on-chip radio-frequency nodes for intra-chip communication) are properly distributed and system optimization is performed in terms of both test application time and test control cost.

Topic Category: System-on-Chip (SOC) Test, System Testing, Test Resource Partitioning

1 Introduction

System-on-chip (SoC) design becomes the trend of IC design, where the entire system is built by reusing pre-designed, pre-verified IP cores. Embedded with these IP cores, a SoC can be viewed as an interconnected network of various functional modules. This new design style shortens time-to-market while meeting various design requirements, such as high performance, low power, and low cost, compared to the traditional system-on-board (SoB) design. At the same time, however, embedded core-based SoC test becomes a challenging task due to IP protection. In particular, there are three major issues to be addressed in SoC test: (1) a

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test access path needs to be constructed for each core to propagate test stimulus and collect test responses, (2) one needs to partition test resources and schedule IP cores to achieve maximum parallelism, and (3) a test control network is needed to initialize different test resources used in the test application and observe the corresponding test results at appropriate instants. The first two issues have been extensively studied in the literature [1] - [9]. In this paper, we focus on a distributed control architecture based on the recent development in “radio-on-chip” technologies.

Currently, the control network connects the central controller (system level controller) with the local control mechanisms by wires in one of the three structures: star, bus, and multiple bus. A system level controller is used to execute the test application based on a predetermined schedule. With continued scaling of microelectronics, a future SoC will see several hundreds of embedded components in a single package and today’s SoC will become tomorrow’s IP core. According to ITRS’99 [10], silicon ICs are to have a chip size of approximately 4cm by 2.5cm and an operating frequency close to 20GHz by 2010. As chips increase in size and complexity, the existing test control models based on direct or bus interconnects are rather limited in not only the accessibility to deeply embedded cores but also the bandwidth limitation of SoC testing. Although copper/low k materials have been introduced for deep sub-micron interconnects, they may become insufficient as the technology goes less than 100nm. Recent studies have shown that the traditional hard-wired metal interconnect system will eventually encounter fundamental limits and may impede the advances of future ultralarge-scale integrated systems (ULSIs) [11].

A new RF/Microwave interconnect technology has been brought forward in ITRS’01 [12]. Integrated with tiny antennae, receivers and transmitters onto a single chip, the chip-based wireless radios can replace the wires (used in the conventional control network) to increase accessibility and improve bandwidth utilization and eliminate delay and cross-talk noise in the conventional wired interconnects. Based on this “Radio-on-Chip” technology, we introduce a novel test control network to transmit control signals chip-wide by radio frequency (RF) links. A number of RF nodes are distributed in the chip to carry control signals. We propose three test control architectures, namely, miniature wireless LAN, multihop scheme, and distributed hierarchical multihop scheme. We also address the control constrained resource partitioning and resource distribution issues in the paper.

In the following, we first briefly overview some test control models and the applicability of intra-chip wireless interconnects in Sec. 2. Then in Sec. 3, we present three types of the new wireless test control architectures: miniature WLAN, multihop scheme and distributed multihop scheme. The formulation of control constrained test resource partitioning and distribution is described in Sec. 4 to minimize the overall testing cost. Finally, Sec. 5 concludes the paper and presents the future work.

2 Related Work

Most test control schemes [13] - [16] use a hierarchical test control methodology employing distributed controllers. Standard interfaces are used for communication between the control units at different levels of the hierarchy. [13] proposes a hierarchical test control architecture, within which each module is associated with a STU (self-testable unit). A hierarchy of supervisors is used to control the test of the entire chip in a way that the top level supervisor communicates with the ATE and controls the lower level supervisors which in turn control the STUs. In [14], three types of hierarchical test controllers provide a structured division of control functions: external BIST access port, BRCs (BIST Resource Controllers) and a distributed BIST control network, which results in uniform and simplified interface protocols between three control levels. Hierarchical test models for core-based system-chips are introduced in [15, 16], which are capable of testing not only JTAG (IEEE 1149.1) cores and CTAG (IEEE P1500) cores, but also the hierarchical cores (cores integrated in a hierarchical fashion). Note that, a vast majority of SoC interconnect networks are using a mix of buses and various forms of point-to-point data or control links. As we mentioned before when moving into the billion transistor era, transmitting signals chip-wide through wires becomes more difficult.

Recently, the concept of using an on-chip network as the fundamental communication architecture for a complex SoC design has been proposed in [17, 18, 19]. To surpass the fundamental limitation of conventional hard-wired interconnects, [11] has introduced a RF/wireless interconnect for future inter- and intra-chip communications, which is based on capacitive coupling, low loss and dispersion-free microwave signal transmission, and modern multiple-access algorithms. With the integration of tiny antennae, receivers and transmitters, an intra-chip wireless interconnect system is proposed in [20] for clock distribution at a chip distance of 5.6mm. As the technology accelerates, new interconnect techniques (such as RF) and on-chip micro-networks (μNetwork) need to be introduced and developed for test connectivity and communication. Moore et al. [21] have applied for the first time, the concept of wireless technique for on-wafer testing. In this paper, we propose a test control network using intra-chip wireless links and accordingly new wireless test control architectures will be presented.

3 Proposed Test Control Architectures

In this section, we first introduce the basic network components. Then we present three proposed test control architectures.

3.1 Network Components

Three basic components are used in the proposed test control architectures: the test scheduler, the resource configurators and the RF (radio frequency) nodes dispersed on the SoC. The test scheduler is employed as a central controller, it (1) carries out the chip level test procedure, including the testing of the interconnects between the cores, the testing of the user-defined logics around the cores and the core testing, (2) communicates with the resource configurators and also with the chip external, such that no conflict arises during resource utilization and test application, (3) configures the routing of the test control path for each individual core, and (4) provides proper test control signals to carry out the test procedure of the selected core. The function of the resource configurator is to configure the test resources required for testing a particular core on command of the scheduler. A set of test resources (i.e., the circuit blocks required to perform testing) is distributed in the system for testing the cores. At any particular control step, each resource is configured into its appropriate operating mode by the control signals. In case when more than one tests share common test resources, the resource configurators are activated such that no conflicts result in the use of resources. The RF node is a radio-frequency interface for (two-way) communication between the scheduler and IP cores. Particularly, one RF node is dedicated to the scheduler. The distribution of RF nodes chip-wide provides the coverage of the entire on-chip wireless communication. To reduce the routing cost and area overhead, one RF node is shared by a cluster of cores which are hard-wired to it. For example, as shown in Figure 1, cores c_1, c_2, c_3 and c_4 are organized into one cluster and are wired to the RF node. In addition, the IP cores in the system are organized into clusters and each has the IEEE P1500 wrapper interface to switch between different modes according to the control signals received.

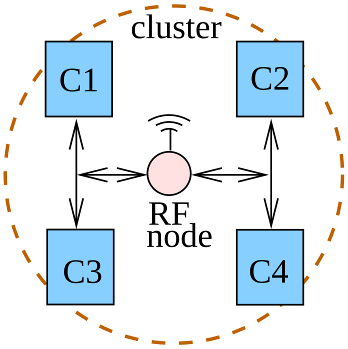

Figure 1: A RF node in a cluster of cores.

3.2 Miniature Wireless LAN Based Test Control Network

Our first proposal is a miniature wireless LAN (local area network) that works as the intra-chip test control network for system-chips, where the scheduler broadcasts control signals through the attached RF node as shown in Figure 2. A single wireless channel is shared by all RF nodes in the chip and the control signals sent from the scheduler will be received by all RF nodes. Each RF node has a unique ID and each control signal is attached with an ID field to specify the intended recipient. Upon receiving a signal, a node checks the ID field through its local decoder. If the signal is intended for the receiving node, the node processes the control signal, otherwise, it is just ignored. By specifically assigning the ID (for example, reserving one bit to indicate multicasting while the remaining bits are to hold a group number), we can also support multicasting to a subset of RF nodes and consequently a subset of cores can be tested concurrently.

When a core finishes testing, the related RF node needs to notify the scheduler its completion. Since the schedule of the tests is predetermined, each RF node is given exclusive access to the network in a predetermined order. Permission to transmit signals to the scheduler is passed from one RF node to another using a special message called a poll and the polling order is maintained by the scheduler according to the schedule result. When the scheduler receives the completion signal from the RF node which holds the poll, it then forwards the poll to the next node in the polling sequence. This centralized polling scheme has its unique features as compared to the conventional polling network, which divides time into alternating types of intervals: polling intervals, during which the poll is transferred between stations, and transmission intervals, during which the station with the poll transmits packets. Our scheme is quite simplified due to the fact that the scheduler knows in advance the completion time of each test and the transmission time is quite short. Thus it's not necessary to maintain the polling and transmission intervals. By using the polling scheme, no collision occurs even when multiple tests finish testing at the same time.

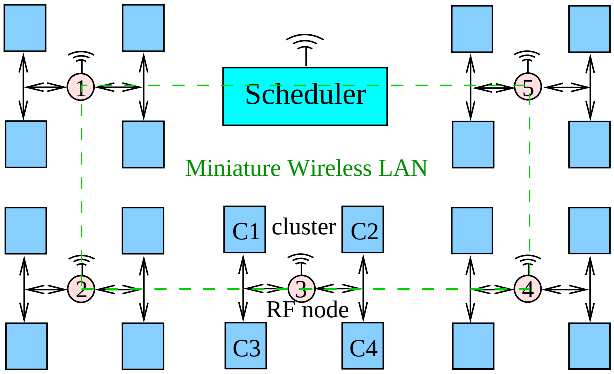

Figure 2: Miniature wireless LAN based architecture.

3.3 Multihop Test Control Scheme

With the simple design of miniature WLAN, all RF nodes should be within the transmission range of the controller. Since the transmission power grows with the transmission range to the power of 2 to 4, relaying signal between RF nodes may result in lower transmission power than communicating over large distance. In addition, the heat dissipated by higher power transmission may damage the surrounding circuits. Therefore, we propose a new low-power, high efficiency multihop scheme, where some RF nodes communicate through multiple "hop" routing.

Due to the limited transmission range of wireless network interfaces, multiple network "hops" may be needed for one RF node to exchange data with another across the network, we name this kind of network as **Multihop Wireless Test Control Network (MTCNet)**. For instance, as shown in Figure 3, since only RF nodes 1 and 2 are within the direct wireless transmission range of the scheduler, the transmission of the control signals between node 3 (or 4) and the scheduler is through the node 1 (or 2). Clearly, some nodes (for instance, node 1 or 2) operate not only as a host but also as a router, forwarding signals to other clusters in the network.

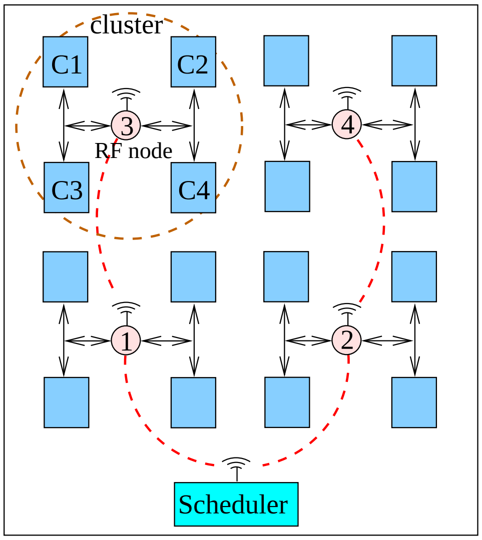

Figure 3: The basic multihop architecture.

In MTCNet, a routing protocol is needed to route the control signals over several hops to its destination. The existing routing protocols such as distance vector and link state for static infrastructure networks, or dynamic source routing (DSR) and ad hoc on-demand distance vector (AODV) for wireless ad hoc networks [22] cannot be directly used here, because all of them rely on powerful and complex hardware support, while a RF node is only a tiny wireless interface. A simplified but efficient routing protocol is needed for effective transmission in MTCNet.

In this paper, we consider geometric routing, which involves wireless links between RF nodes and the scheduler, and hard-wiring between RF nodes and dedicated cores. In MTCNet, the location of the cores and resources are fixed, and the placement of the RF nodes is predetermined (see Sec. 4). In such a static network, two issues need to be addressed with regards to routing. First, the cores need to be properly clustered such that the cost for hard-wiring a core to the RF node within its cluster is minimized. Core clustering depends on core functionality and resource sharing, and is determined before test scheduling. Second, an efficient topology needs to be formed such that the degree of each RF node (the number of neighbors with direct wireless links) should be small. Here, the topology is defined as the set of RF links between node pairs used explicitly by a routing mechanism.

We propose a source routing approach for the communication between the RF nodes, where the scheduler specifies the route that a control signal should take through the network. More specifically, the scheduler maintains a routing table recording the shortest routes between any node and the scheduler, and works as the central node to make routing decisions. A shortest path algorithm (for example, Dijkstra's algorithm [23]) is needed to find the shortest route to any RF node in the network from the scheduler. The idea is to build a graph of the network, with each vertex representing a RF node and each edge between two nodes representing a wireless link, and the RF node attached with the scheduler is defined as the source. The shortest route between any destination and the source is found by running the shortest path algorithm on the graph. Each RF node is assigned a unique ID, and each message carries in its header the complete ordered list of node IDs through which the signal must pass. The scheduler put the entire route into the header when sending a control signal. The intermediate nodes check the header and forward the signal to the next hop accordingly.

3.4 Distributed Multihop Scheme

In order to improve parallel test control processing, we propose an advanced hierarchical multihop scheme. In this architecture as shown in Figure 4, the scheduler is the system controller controlling a set of subsystem controllers which are distributed within the transmission range of the scheduler. Each subsystem includes a number of clusters and has a similar architecture as the basic network as shown in Figure 3. In this multilevel tree structure, the system controller will send the control information to the subsystem controllers which in turn control their subnetwork, such that efficient parallel communication is achievable. However, introducing a hierarchical level of controllers increases the test control overhead. In order to well balance the tradeoff between test application time and test control cost, the number of subsystem controllers usually equals to the maximum number of tests in a concurrent test set (within which all tests can be executed in parallel). Thus, the tests that are simultaneously interrupted are processed by different subsystem controllers.

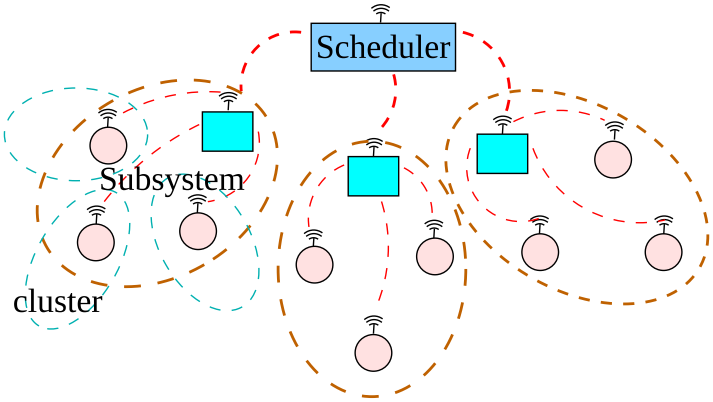

Figure 4: The distributed multihop architecture.

4 Control Constrained Resource Partitioning and Distribution

Various test scheduling and wrapper/TAM optimization algorithms have been proposed in the literature to reduce test cost in terms of test application time. However, less attention is paid to test control cost which constitutes a major part of the total test overhead. In this section, we propose a system optimization scheme to minimize the combined cost of overall testing time and test control under power constraint and resource conflict. We assume that a hierarchical multihop test control architecture is used to achieve the most possible parallelism.

4.1 Test Control Overhead & Resource Partitioning

The test control cost in the system mainly includes the number of subsystem controllers and their complexity, the distribution of resources (including not only the circuitry to perform testing but also the RF nodes) and routing cost (including wireless routing as well as hard-wiring among clusters). The impact of test control overhead on the overall testing cost is briefly discussed below.

In order to minimize the overall testing time, nonconflicting test sets (i.e., there's no resource conflict between them and their total power meets the maximum power limit) are executed in parallel. A schedule for a system is made up of a set of test sessions, each consisting of a set of power-constrained concurrent test sets (PCTS) [3]. Corresponding to each PCTS, a set of controllers is needed to issue a set of control signals to parallel-process the controlling and these control signals are routed along different paths. Each control signal drives different test resources required for dedicated cores in the same PCTS. This directs the partitioning of the test resources, where each partitioning would be driven by the same set of control signals. Thus the test resources driven by the same control signal would be physically adjacent to each other.

Due to parallel controlling, the number of controllers relies on the maximum number of tests (size of a PCTS) in the PCTS's. Different scheduling will result in different size of PCTS's and in turn requires different number of controllers, and vice versa. Moreover, the complexity of each controller depends on the number of control signals it needs to generate. The number of control signals required to execute a test may vary from one to another. Hence, the lower the disparity in the number of control signals that are necessary for different test sets in the same PCTS, the more cost-efficient is the controller.

The wiring cost can be significantly reduced if the cores sharing the same resources are physically adjacent. Thus the clustering of cores is performed according to their physical locations and the sharing of resources. Further, the clustering also depends on the placement of RF nodes (which will be discussed in the next subsection) as each RF node covers the communication of a cluster of cores. Note that different partitioning of test resources and RF nodes may result in different clustering of the cores which affects the concurrency relation between the cores, and accordingly different test schedules. Thus the reduction in the test application time does not necessarily imply the reduction in overall testing cost. In addition, as the cores within a cluster are adjacent to each other, the wiring cost is properly reduced, and the routing cost is mainly determined by the number of RF nodes for constructing an efficient topology. In summary, reduction in test control overhead should aim at proper partitioning of overall resources (including not only the testing resources but also the communication resources) and the concurrent scheduling of tests.

4.2 The Placement of RF Nodes

Given a SoC embedded with n cores and m resources, a tentative floor plan, and the maximum assistant distance of the RF node R (the maximum range for connecting a core to the RF node) , the resource distribution problem is deduced to find the minimum number of RF nodes needed to cover the communication of all cores within the chip and their placement.

This problem can be formulated into geometric disk covering [24, 25], where a (clustered) wireless control network can be abstracted as a set of disks, each centered at a RF node with a radius of R, that covers a set of embedded IP cores (wireless clients) in the chip plane. A graph $G(V, E)$ is used to represent the system. V is a set of vertices, each representing an embedded IP core. E is a set of edges, each connecting two vertices within a distance of $2R$. Assuming an optimally placed RF node can assist at least two IP cores, i.e., a disk covers at least two vertices, we can always move the RF node such that there are two vertices on the circumference of the disk, while the disk covers the same set of vertices (see Figure 5(a)) [25]. For each edge, a RF node can be placed in two ways such that the two vertices connected by the edge are on the circumference of the disk (see Figure 5(b)). Thus there are maximum $2|E|$ possible RF node placements need to be considered. For each RF node placement, the node position (X_i, Y_i) $(1 \leq i \leq 2|E|)$ can be computed accordingly, and the corresponding disk covers a set of vertices, denoted as set S_i. Therefore, the original problem becomes the set covering: select a minimum of K sets from the $2|E|$ sets to cover all IP cores in the chip with each set is assisted by one RF node. The set covering problem is proven to be a NP complete problem [23] and efficient heuristic algorithms [26] exist to solve it.

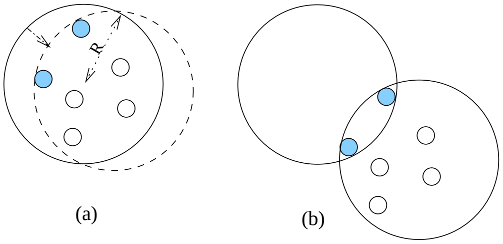

Figure 5: The illustration of disk covering.

5 Conclusion and Future Work

In this paper, we have proposed a novel distributed wireless test control network using the “radio-on-chip” technology for future high density, high volume embedded system chips. Three types of control architectures, i.e., miniature WLAN, multihop scheme and distributed multihop scheme have been presented and the system optimization has been performed on control constrained test resource partitioning and distribution. In future research, several system optimization issues such as RF nodes placement, the optimal number of RF nodes and routing problems will be addressed in detail under the multilevel tree structure. Techniques need to be presented for the integration of test resource distribution and system optimization among TAM design, test scheduling (concurrent core testing as well as interconnect testing) under power and cost constraints. Simulations using randomly generated test sets and experiments with benchmarks will be performed for evaluation and verification of the proposed test optimization algorithms.

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