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Reconfigurable missile-borne SAR imaging SoC design

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Abstract: With the rapid development of the integrated circuit manufacturing technology and the radar technology, the demand for miniaturisation, low power consumption, and real-time performance of synthetic aperture radar (SAR) imaging system is becoming higher and higher. By designing reconfigurable IP cores and configuring parameters through CPU, a reconfigurable missile-borne SAR imaging SoC chip based on IP reuse is designed to meet this urgent demand. Using 0.13μm CMOS process, the SoC chip has been taped out and verified successfully. Compared with the traditional 'DSP + FPGA' platform, this chip can ensure the real-time performance of the missile-borne SAR imaging system and has more advantages in scale and power consumption.

1 Introduction

SAR is an all-weather microwave remote sensing technology [1, 2]. By emitting large time-bandwidth radar signals, the pulse compression processing technology for radar echo data can obtain high range line resolution, and the relative motion which can form an equivalent synthetic aperture antenna array between radar platform and target can obtain high azimuth line resolution. Therefore, SAR imaging systems can provide high resolution and high precision two-dimensional images.

With the development of radar technology, the SAR imaging technology is widely used in the missile-guidance system [3–6]. The missile-borne SAR imaging system has certain requirements of miniaturisation, low power consumption, and real-time performance, and usually needs to work in many different modes. Due to the complexity of the missile-borne SAR imaging algorithms, the volume of the radar imaging system is usually very huge, with high power consumption and cost, which is increasingly not suitable for the development of the missile technology.

The SAR imaging system usually uses high performance FPGA and DSP chips for signal processing [7–11], which is not as good as the application-specific integrated circuit (ASIC) in the aspects of real-time, reliability, small-scale and low power consumption. Taking a commonly used SAR imaging system as an example, the whole system is made up of two PCB boards. As shown in Fig. 1, the main computing unit consists of many foreign high-end FPGA and DSP chips, with a large-scale and a total power consumption of over 100 W. Using TMS320C6678 of TI as DSP with the image size of each frame is 8192 × 2048 × 64, the operation time of a 8 K floating-point FFT is about 0.48 ms when the operating frequency is 100 MHz, which means that the system's real-time performance cannot be guaranteed. Therefore, with the improvement of the integrated circuit technology, the ASIC design method which can integrate CPU, all kinds of interfaces and key IP cores on a single chip, can effectively meet the requirements of SAR imaging applications.

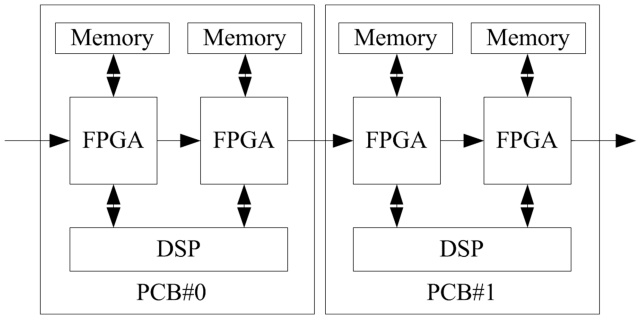


Fig. 1 *SAR imaging system hardware topology*

In order to improve the performance of SAR imaging system, there are many good solutions based on improved algorithms [12–17]. However, according to the trend of the missile-borne SAR imaging system, this paper presents a reconfigurable missile-borne SAR imaging SoC chip based on IP reuse, which can be applied to most of the FFT-based SAR imaging algorithms. Several reconfigurable IP cores have been designed. By configuring parameters through CPU, reconfiguration in and among modules will be done to control data flow and implement different functions. Meanwhile, the main data flow will not pass through the CPU to reduce the workload of CPU and improve the real-time performance of the system.

The rest of this paper is organised as follows. Section 2 introduces the processing of the missile-borne SAR imaging signal. Then, the reconfigurable missile-borne SAR imaging SoC design is given in Section 3. Section 4 presents a board-level verification platform and its simulation results. Finally, conclusions are drawn in Section 5.

2 Processing of missile-borne SAR imaging signal

Take the side-looking Range-Doppler (RD) processing algorithm with motion compensation as an example, while the size of each raw-echo frame is 8192 × 2048, and the size of each SAR-image frame is 4096 × 2048. The real part and the imaginary part of each data are both 32-bit-wide. As shown in Fig. 2, the processing of the missile-borne SAR imaging signal includes four steps:

i. Range line pulse compression: Before node 1, the range line FFT (8K-point) transform is applied to the raw echo data, then the transformed data are multiplied by the pulse compression matching function (PCMF) and the linear phase function (LPF) to correct range walk. Finally, the range line IFFT (8K-point) transform of the compensated data is performed.
ii. Parameters estimation based on motion compensation: According to the need of image processing, the data output by the range line pulse compression are truncated to 4096×2048 in range line, then divided into many blocks in azimuth line to estimate the Doppler frequency rate (Fdr) with the Correlative Function method [8] and the Doppler centroid frequency (Fdc) with the Map Drift method [18]. The Fdr is used for the Doppler rate error compensation based on the range line matching function (RMF), and the Fdc is used for the Doppler centroid offset compensation based on the azimuth line matching function (AMF), respectively.
iii. Second range line compensation: Compensation for the Doppler rate error in frequency domain between node 1 and node 2. According to the need of image processing, the data output by the range line pulse compression are truncated to 4096×2048 in range line too. Therefore, the point number of the corresponding FFT and IFFT is 4 K.
iv. Azimuth line deformation correction: Compensation for the Doppler centroid offset in frequency domain and correction for the azimuth line deformation between node 2 and node 3, after which the final SAR images can be output. The corresponding point number of the FFT and IFFT is 2 K due to matrix transpose between the range line and the azimuth line.

The Doppler rate and the Doppler centroid are estimated when the amount of echo data is corresponding to the size of the SAR image. Meanwhile, matrix transposes are necessary for the SAR imaging system between range line and azimuth line switching. The place where the data need to be transposed is shown in Fig. 2 by node 2. The real-time performance of the main data flow is affected by FFT, IFFT, matching function, memory access efficiency etc.

3 Reconfigurable missile-borne SAR imaging SoC design

In order to ensure the miniaturisation and real-time performance of the SAR imaging SoC chip, this paper has designed several reusable reconfigurable IP cores to save hardware resources, and a dedicated memory management unit (MMU) to improve memory access efficiency. The operation of main data flow will be implemented in the ASIC way to improve the operation speed. Finally, by configuring parameters through CPU, the process of the side-looking RD algorithm with motion compensation shown in Fig. 2 will be finished through a few hardware resources.

3.1 Reconfigurable IP cores

3.1.1 FFT/IFFT: There are a total of four times of FFT operation and three times of IFFT operation in Fig. 2. For pipeline processing, nodes are usually partitioned according to the needs of data storage, such as the three nodes in Fig. 2. According to the process of the side-looking RD algorithm, if IP cores can be reused, only two FFTs and one IFFT are needed.

This paper designs a floating-point high-speed FFT/IFFT core based on mixed radix-2/4, as shown in Fig. 3. There are several optional parameters, such as time and frequency domain selection (DIT/DIF), forward and inverse transform selection (FFT/IFFT), point number (NFFT), and precision (PRE). These parameters are configured by CPU timely to achieve different functions and meet the IP reuse requirements.

3.1.2 Arithmetic acceleration unit (ACU): During the process of the side-looking RD algorithm with motion compensation, there are many phase compensation operations. In order to simplify these arithmetic logic operations, a reconfigurable arithmetic unit has been specially designed to accelerate the operations. The

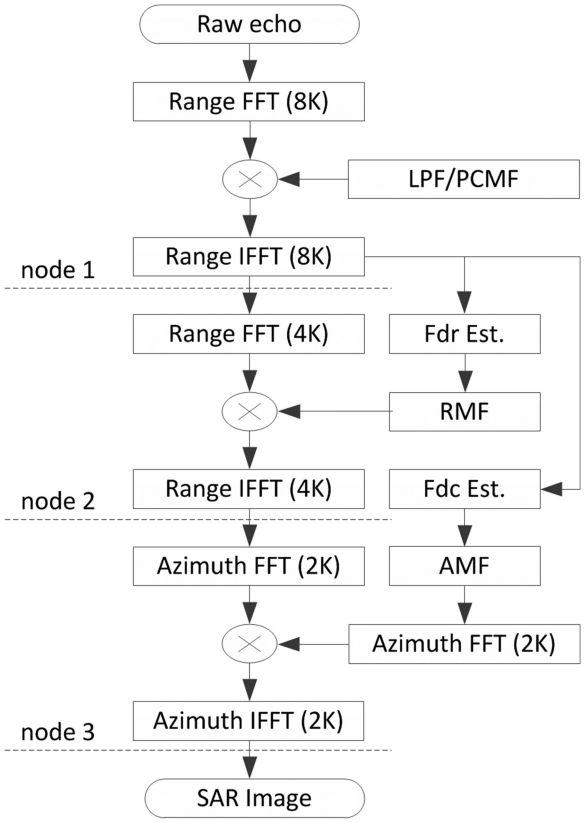


Fig. 2 *Process of the side-looking RD algorithm with motion compensation*

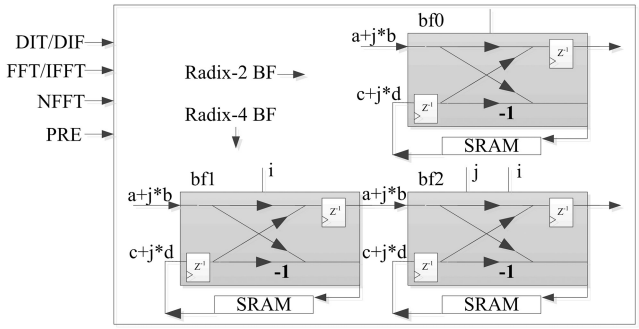


Fig. 3 *Floating-point high-speed FFT/IFFT core based on mixed radix-2/4*

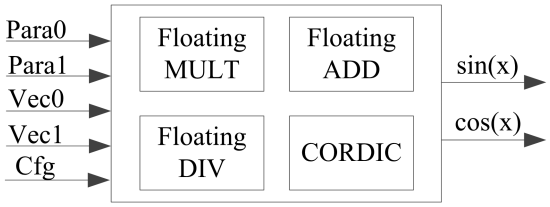


Fig. 4 *Architecture of the ACU*

compensation factors of the matching function can be summed up as formula (1).

$$\exp(j \times \text{Para0} \times [\text{Vec0} - \text{Vec1}/\text{Para1}]) \quad (1)$$

This formula is realised by the ACU shown in Fig. 4, in which Para0 and Para1 are scalars, **Vec0** and **Vec1** are vectors.

First, the intermediate variables (Para0 and Para1) are calculated in advance by CPU based on the operational expressions and system inputs. Then, the vectors (**Vec0** and **Vec1**) required for phase compensation are directly generated or calculated in advance by CPU in accordance with a specific rule. Finally, the trigonometric functions are completed by pipeline operation of

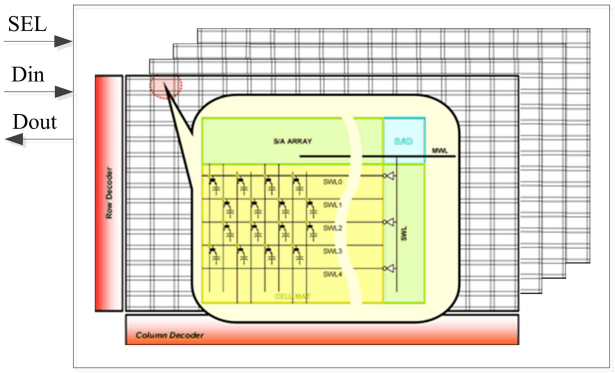


Fig. 5 *3D architecture of SDRAM chip for MMU*

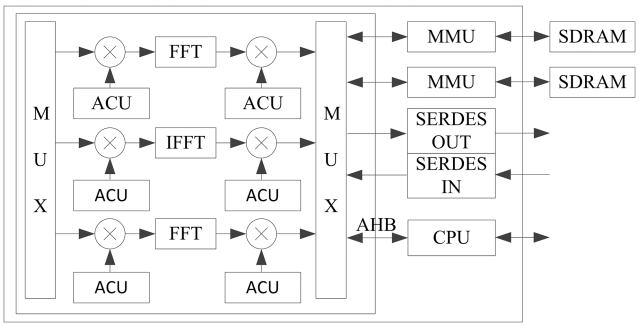


Fig. 6 *Architecture of the reconfigurable missile–borne SAR imaging SoC*

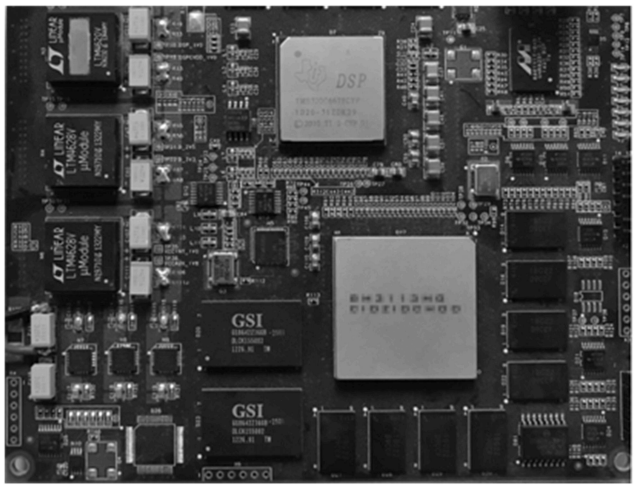


Fig. 7 *Verification platform of the proposed SoC chip*

CORDIC. The results are output to multiplicative modules shown in Fig. 2. In order to be more flexible, the internal computing units are all interlaced and interconnected, and the configuration bit Cfg of the switching points is configured timely by CPU, as shown in Fig. 4.

3.1.3 MMU: The data access efficiency and the matrix transpose efficiency of memory have great influence on the real-time performance of SAR imaging system, since node 1 and node 2 shown in Fig. 2 are all required to store a large number of data. In order to improve the memory access efficiency, a dedicated MMU is designed based on the characteristics of SAR imaging data flow.

As a commonly used external memory for SAR imaging system, the three-dimensional (3D) architecture of SDRAM chip is shown in Fig. 5 [19, 20]. The memory is distributed not only by row and column, but also divided into very small blocks. In order to make full use of the data bus cycles, data access is achieved through data interleaving pattern among sub-blocks. The MMU work mode can be configured through the SEL port in Fig. 5, selecting the sequential access operation required by node 1 or selecting the transposed operation required by node 2.

Table 1 Performance of different floating-point FFTs

Processor	Point number, K	Frequency, MHz	Execution time, μs
MPSoC [22]	8	400	41.7
TS201 [23]	8	600	903
TMS320C6678 [24]	8	1250	38.3
The proposed SoC	8	100	82.7
	4	100	42.3
	2	100	21.4

3.2 Architecture of the reconfigurable missile-borne SAR imaging SoC

Based on the proposed reconfigurable IP cores, the architecture of the reconfigurable missile-borne SAR imaging SoC is shown in Fig. 6, including one CPU, two FFTs, one IFFT, six complex multipliers, six ACUs, two MMUs etc. For continuous images processing, this paper adopts two MMUs and two external SDRAM chips to realise ping-pong storage operation. Data transmission is accomplished by the high-speed serial circuits SERDES.

According to the processing flow shown in Fig. 2, the detailed working process of the SoC chip is as follows:

i. Power on and initialise the chip, then configure the parameters through CPU to determine the function of the reconfigurable IP cores and the direction of the data flow.
ii. Execute the range line pulse compression operation and the estimate motion compensation parameters at the same time.
iii. Reconfigure the system parameters and complete the second range line compensation operation according to the Doppler rate.
iv. Reconfigure the system parameters and complete the azimuth line deformation correction operation according to the Doppler centroid.
v. Output SAR images.

In summary, the main data flow does not pass through the CPU to reduce the workload of CPU and improve the real-time performance of the system. Meanwhile, in order to save logic resources, a customised floating-point arithmetic unit with suitable precision and dynamic range has been used in the proposed SoC chip.

4 Board level verification

The proposed SoC chip has been taped out and verified successfully. The verification platform is shown in Fig. 7. Using 0.13 μm CMOS process, the chip area is 13 mm × 13 mm. The size of each raw-echo frame is 8192 × 2048, and the size of each SAR-image frame is 4096 × 2048. Each data are 64-bit-wide. According to the SAR imaging system requirements, the interval between the input data per range line is not <145 μs. Meanwhile, in order to evaluate the SAR image quality of the proposed SoC chip, this paper adopts commonly used spatial resolution, peak-side lobe ratio (PSLR), and integrated-side lobe ratio (ISLR) for point target, and radiometric resolution for distributed target [21].

As shown in Fig. 2, FFT and IFFT are the key modules which have a great impact on the real-time performance of the RD algorithm. Since the operation time of FFT and IFFT are almost the same, this paper compares the performance of different floating-point FFTs among the proposed SoC chip and several processors, as shown in Table 1. If working at the same frequency and with the same point number, the speed of the proposed reconfigurable FFT core is the fastest.

Table 2 shows the execution time for each step in Fig. 2. As shown in Fig. 2, step 1 and step 2 are performed in parallel, and step 2 requires pulse compression data from step 1, so the execution time of step 1 is a little bit smaller than step 2. At the same time, in addition to the complex multipliers shown in Fig. 6, other modules such as ACU and MMU are executed in parallel

Table 2 Execution time for each step

Step	Execution time, ms
range line pulse compression	296.9
parameters estimation	297
second range line compensation	86.7
Azimuth line deformation correction	87.8

Table 3 Performance of the proposed SoC

Frequency, MHz	Power consumption, W	Image processing time, ms/frame
200	8.95	235.8
100	4.98	471.5
50	2.64	943

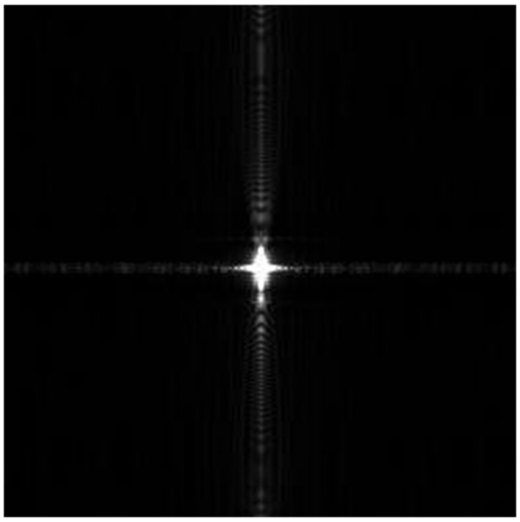
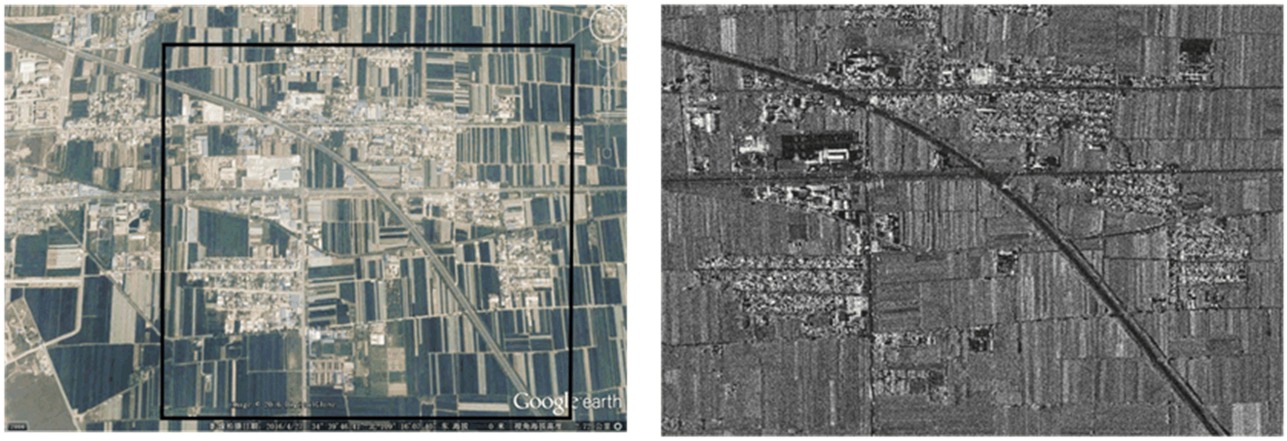


Fig. 8 *Single point target (256 × 256)*



a *b*

Fig. 9 *Effect drawing display for distributed target*
(a) From Google earth, ***(b)*** From the proposed chip

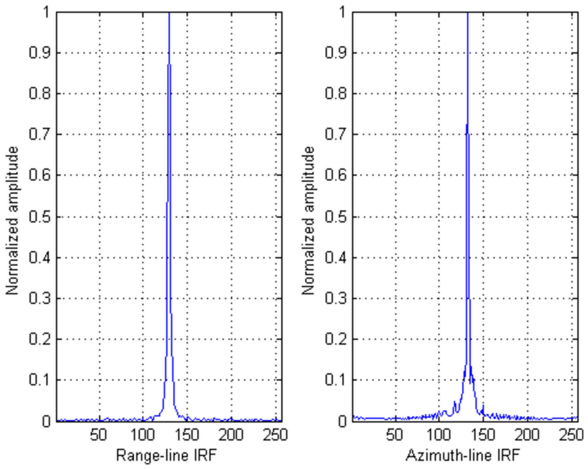


Fig. 10 *IRFs of the point target in both range-line and azimuth-line*

with FFT and IFFT without additional image processing time. Thus, the total execution time for each frame is 471.5 ms, the execution time of step 1 is not taken into account.

Table 3 shows the power consumption and the image processing time per frame of the proposed SoC at different frequencies. The power consumption is 4.98 W and image processing time is 471.5 ms per frame when the operating frequency is 100 MHz. Meanwhile, higher frequency will lead to excessive power consumption, while lower frequency will affect the real-time performance of the SAR imaging system. Therefore, the proposed SoC chooses 100 MHz as its common working frequency.

In order to evaluate the SAR image quality, a point target shown in Fig. 8 and a distributed target shown in Fig. 9 are analysed here. The impulse response functions (IRF) of the point target in both range-line and azimuth-line are in the form of $|\mathrm{sinc}(x)|$ function in time domain [25], as shown in Fig. 10. The size of the analysed area is 256 × 256, since the point target is located in a very small area. The corresponding evaluated results for image quantity are shown in Table 4, which means that all three parameters can meet the SAR imaging system requirements.

Table 4 Point target evaluation result

	PSLR, dB	ISLR, dB	Spatial resolution, m
range-line	−18.61	−16.41	2.5
Azimuth-line	−17.65	−13.76	3
system specification	≤−16	≤−13	5

For Fig. 9, the image displayed in Google earth which is on the left side and the real image obtained from the actual flight test of a cruise missile-borne SAR imaging system which is on the right side are analysed. The raw-echo data which size is 8192×2048 is sampling in the cruise phase of the cruise missile. The size of the SAR-image frame is 4096×2048. Using the side-looking RD processing algorithm shown in Fig. 2 with the operating frequency is 100 MHz, the proposed SoC chip takes a time of 471.5 ms to complete an image processing, which is suitable for missile-borne SAR imaging system. Meanwhile, the corresponding radiometric resolution for the area shown in Fig. 9*b* is 2.83 dB, and it can be found from the output SAR image that the characteristics of each target in the image are obvious.

5 Conclusions

Integrating CPU, all kinds of interfaces and key IP cores on a single chip is in accordance with the development of missile technology. With lower power consumption and smaller scale compared with the traditional 'DSP + FPGA' platform, the proposed SoC chip can ensure the miniaturisation, low power consumption, and real-time performance of the SAR imaging SoC system. By designing several reconfigurable IP cores and configuring parameters through CPU, the FFT-based SAR imaging algorithms can be implemented flexibly. Besides, the testing results show that the speed of the proposed reconfigurable FFT core is the fastest compared with other processors, and the real image obtained from the actual flight test is very perfect. Furthermore, this design can be used as a universal SAR imaging SoC design method and will be widely used in the missile-borne SAR imaging system.

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