VLSI Systems and Embedded Architectures

Ramalingam Sridhar
High Performance VLSI Systems & Architecture Laboratory
215 Furnas Hall
Dept of Computer Science & Engineering
University at Buffalo
Email: rsridhar@cse.buffalo.edu
Automation

- Process Automation
- Office Automation
- Home Automation
- Automobile Automation
Home Automation

- Fully wired environment
- Standards emerging
- Network standard for Home Audio/Visual electronics that will connect seamlessly and interoperate
- Appliances control standard (networked appliances)
- Phone line standards & network protocol for multiple computers to share peripherals and a single internet connection
- Set top TV Boxes
Automobile Automation

• Mobile environment with in-vehicle networks with internet, wireless links, personal communication devices, entertainment electronics and traditional car systems converge

• Integration of GPS into various functions

• Digital systems with 100Mbps network for video will be a requirement.

• Embedded systems have already transformed an automobile

• Automobile Multimedia Interface Collaboration (AMIC)
Environment
Basic Requirements for Software

- Portability (external application software)
- Interoperability (remote service, network adaptation)
- Processing Architecture Flexibility
- Failsafe Operation
- Security
- Plug and Run(Play)
- Upgradeability
- Serviceability
- Internationalization Support
- Functions of API
Embedded systems

- Embedded processors and control hardware
- Remote diagnostics of appliances and devices
- Easy access to vast database of knowledge
- Science fiction scenario is now a reality
Enabling Technologies

- Sensors
  - Used extensively in automation, in particular in automobiles
- Integration of Sensors with conventional electronics
- Extraordinary computing power on the palm tip is possible by the extraordinary progress in VLSI Technology
Moore’s Law

- Predicted that number of transistors per chip would grow exponentially (double every 18 months).
- Exponential improvement in technology is a natural trend: steam engines, dynamos, automobiles.
Moore’s Law

* In 1965 Gordon Moore predicted that the number of transistors on processors would double every two years. His prediction has proven remarkably accurate so far.

Source: Intel, VLSI Research, Inc.
## Silicon in 2010

- **Die Area:** 2.5x2.5 cm²
- **Voltage:** 0.6 V
- **Technology:** 0.07 µm

### Memory Devices

<table>
<thead>
<tr>
<th>Device</th>
<th>Density (Gbits/cm²)</th>
<th>Access Time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM</td>
<td>8.5</td>
<td>10</td>
</tr>
<tr>
<td>DRAM (Logic)</td>
<td>2.5</td>
<td>10</td>
</tr>
<tr>
<td>SRAM (Cache)</td>
<td>0.3</td>
<td>1.5</td>
</tr>
</tbody>
</table>

### Gate Array Technologies

<table>
<thead>
<tr>
<th>Technology</th>
<th>Density (Mgates/cm²)</th>
<th>Max. Ave. Power (W/cm²)</th>
<th>Clock Rate (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Custom</td>
<td>25</td>
<td>54</td>
<td>3</td>
</tr>
<tr>
<td>Std. Cell</td>
<td>10</td>
<td>27</td>
<td>1.5</td>
</tr>
<tr>
<td>Gate Array</td>
<td>5</td>
<td>18</td>
<td>1</td>
</tr>
<tr>
<td>Single-Mask GA</td>
<td>2.5</td>
<td>12.5</td>
<td>0.7</td>
</tr>
<tr>
<td>FPGA</td>
<td>0.4</td>
<td>4.5</td>
<td>0.25</td>
</tr>
</tbody>
</table>
## NTRS Adjusted Roadmap

<table>
<thead>
<tr>
<th>SemaTech NTRS</th>
<th>1995 0.35µm</th>
<th>1998 0.25µm</th>
<th>2000 0.18µm</th>
<th>2002 0.13µm</th>
<th>2004 0.10µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>3.3V</td>
<td>2.5V</td>
<td>1.8V</td>
<td>1.5V</td>
<td>1.2V</td>
</tr>
<tr>
<td>Metal layers</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>6</td>
<td>7</td>
</tr>
<tr>
<td>Short wire pitch</td>
<td>0.70 -1.05µm</td>
<td>0.65 - 0.90µm</td>
<td>0.50 -0.80µm</td>
<td>0.35 - 0.65µm</td>
<td>0.20- 0.50µm</td>
</tr>
<tr>
<td>Clock freq.</td>
<td>300 MHz</td>
<td>450 MHz</td>
<td>800 MHz</td>
<td>1 GHz</td>
<td>1.4 GHz</td>
</tr>
<tr>
<td>Interconnect pitch</td>
<td>1.0µm</td>
<td>0.8µm</td>
<td>0.6µm</td>
<td>0.42µm</td>
<td>0.28µm</td>
</tr>
</tbody>
</table>

**Recent announcements (Aug- Sep 98)**
* TI - 0.10-micron CMOS, 400 million tx, Volume prodn.- Yr 2001
* Sun Micro UltraSparc III - 600MHz, 70W, 300 mm sq.
VLSI Chip in Year 2005

- Updated International Technology Roadmap:
- Min feature size 0.1 micrometer
- Total no. of transistors 200 million
- Number of logic transistors 40 million
- Clock frequency 2.0-3.5 GHz
### 1998 ITRS Technology Characteristics

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory (Bit per chip)</td>
<td>256M</td>
<td>1G</td>
<td>4G</td>
<td>16G</td>
<td>64G</td>
</tr>
<tr>
<td>Transistors per chip (MPU)</td>
<td>11M</td>
<td>21M</td>
<td>76M</td>
<td>200M</td>
<td>520M</td>
</tr>
<tr>
<td>Pins/Balls (ASIC)</td>
<td>1130</td>
<td>1400</td>
<td>1915</td>
<td>2619</td>
<td>3581</td>
</tr>
<tr>
<td>Chip Frequency (MHz)</td>
<td>750</td>
<td>1250</td>
<td>2100</td>
<td>3500</td>
<td>6000</td>
</tr>
<tr>
<td>Wiring Levels (Max)</td>
<td>6</td>
<td>6-7</td>
<td>7</td>
<td>7-8</td>
<td>----</td>
</tr>
<tr>
<td>Power Supply Voltage (VDD)</td>
<td>1.8-2.5</td>
<td>1.5-1.8</td>
<td>1.2-1.5</td>
<td><strong>0.9-1.2</strong></td>
<td><strong>0.6-0.9</strong></td>
</tr>
<tr>
<td>Power (W)-High performance</td>
<td>70</td>
<td>90</td>
<td>130</td>
<td>160</td>
<td>170</td>
</tr>
<tr>
<td>Power (W)-Hand held</td>
<td>1.2</td>
<td>1.4</td>
<td>2</td>
<td>2.4</td>
<td>2.8</td>
</tr>
</tbody>
</table>
SIA’s “Design Productivity Crisis”

Transistors/chip (without memory)

Transistors designed/staff month


Moore’s Law

Gap

Limit to Adding Skilled Engineers

Engineering Productivity Trend

10/6/99

HPVSA Laboratory, University at Buffalo

Source: Semiconductor Industry Association
The International Technology Roadmap For Semiconductors

The ITRS Identifies Several “Major Roadblocks”

- The ability to continue affordable scaling --
- Affordable lithography at and below 100nm --
- New materials and structures
- Multi-GHz frequency operation on-and off-chip -- timing,
  interconnect, package…
- Metrology and test -- broad spectrum of new approaches are required
- The research and development challenge -- how to organize, how to fund
**MAJOR ROADBLOCKS**

**Affordable Device Scaling**

- Feature sizes must continue to shrink in order to maintain 25-30% per year productivity increase

- Increasing number of transistors per square centimeter and increasing speed presents design and interconnect problems

- Design, test and interconnect become limiting technologies

- Costs and complexity are escalating rapidly
Electronics Industry

- Achieved Successful Penetration in Diverse Domains
High Complexity: Mixed Technologies

- Embed in a single chip: Logic, Analog, DRAM blocks
- Embed advanced technology blocks:
  - FPGA, Flash, RF/Microwave
- Beyond Electronic
  - MEMS
  - Optical elements
Electronics Industry

- Met User **Quality** Requirements
  - satisfying users to buy products *again*

Created an Unprecedented **Dependency**
- market-driven product
  Users want

“**Better, Cheaper, Smaller, Faster**”
Market-Driven Industry Trends

• Cause emergence of SOC Technology:
  Greater Complexity
  Increased Performance
  Higher Density
  Lower Power Dissipation
SoC is Revolutionizing the Electronics Industry
SOC Definition

"Real" Component

System on Board

Component based design

"Virtual" Component

System-on-a-Chip

Courtesy: VSI Alliance
SOC Application Drivers

• Boom in communications, multimedia and consumer electronics

• Examples:
  – CISCO 700 Router: 32-bit MIPS R5000+ ASICs + 6Mb RAM
  – Digital camcorder: 16-bit processor + CCD array + A/D converter + 4-layer board
  – Digital TV, Digital set-top box
  – PC add-on cards (Sound blaster)
System(s)-on-a chip

- SOC introduces reuse of IP blocks
- Due to the complexity of designing the entire chip, the design becomes managing various building blocks and building larger comprehensive chips from these blocks.
- More reliance on the software verification and simulation, than ever before.
System on chip

- System on chip opens the way for a multitude of electronics products not economically feasible before.
- SOC technology holds the key to increasingly complex applications by enabling high-performance, embedded processing solutions at a low, single-chip cost.
SIP Security

- Patents, copyrights, trade secrets, maskworks, trademarks
- Public key cryptography
- License management on networks
- Digital fingerprinting
  - Digital signature for cores
- Watermarking
### DSM - Shift in Problems and Priorities

- **1.0 Micron**
  - Area, Speed
- **0.8 Micron**
  - Speed, Area
- **0.7/.6 Micron**
  - Speed, Area, Power
- **0.5 Micron**
  - Speed, Power, Area
- **0.35 Micron**
  - Speed, Power, Area, metal migration
- **0.25 Micron**
  - Speed, Metal-Migration, Power, Signal-Integrity, Area
- **0.18 Micron**
  - Speed, Metal-Migration, Power, Signal-Integrity, EMI

#### Table

<table>
<thead>
<tr>
<th></th>
<th>1.0</th>
<th>0.8</th>
<th>0.7</th>
<th>0.5</th>
<th>0.35</th>
<th>0.25</th>
<th>0.18</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Speed</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Power</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Metal-Migration</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Signal Integrity</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>EMI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>

**Source:** Dataquest

10/6/99

HPVSA Laboratory, University at Buffalo
“Today it costs about $100 million, or about $16 per transistor, to develop a 6 million transistor chip. In 2005 chips will contain 300-400 million transistors. If productivity remains flat between now and then, developing such chips will cost in the $6-8 billion range... the same cost as developing a Boeing 777.

Hector J. Ruiz, President Motorola SPS
Virtual Prototyping Directions

VERIFICATION
- Formal Verification
- Static Timing

RTL Test

Mixed-Signal Simulation
- Formal Analysis
- VHDL & Verilog Sim
- Cycle-Based Simulation

RTL Test Bench

Emulation

Logic Synthesis

RTL Floor planner

Timing
- Signal-Integrity
- EMI
- Power
- Metal-Migration

RTL Virtual Prototype

Hardware/Software Virtual Prototype

DESIGN

Embedded Software

DFT
Design challenges

- Can the Moore’s law hold good in the future.
- Shrinking transistors => testing the physical limits
- Increasing speed results in increased power
- Achieving low power even with increased speed
- Due to System-on-chip, we have powerful functions including computing designed to the size of a postage stamp, which makes useful and extraordinary mobile applications possible.
Areas of Research

• Digital Systems, Computer architecture & VLSI Systems
  – focus on deep sub-micron design, interconnect issues, silicon IP and low power
  – applications to multimedia, communication and DSP
VLSI Systems

• CMOS Designs
  – low feature size (0.18micron from 3micron in ’85), moving towards 0.1micron
  – input pattern dependence on delays and power
  – dependence on previous states of the output

• Deep sub-micron designs
  – reaching physical limitations
  – better modeling & simulations
Power consumption in CMOS
- Supply voltage; threshold voltage
- speed
- switching

Power minimization at higher level
- instruction reordering
- compiler level optimization & algorithmic modifications
Interconnect issues

• Dominance of Interconnect wires in determining the performance
• logic-based design emphasis to interconnect wire based design
• routing, placement and delays impact the performance
• Clock distribution networks and skews
Interconnects

- Architectural design impact due to interconnect dominance
- Clocking and synchronization issues
- Synchronous and asynchronous interface
Silicon IP

• System on a Chip (SOC)
  – mobile phones and powerful gadgets
  – Example: DSP, processor, communication modules; RF circuit blocks all in a cell phone
• Encryption, watermarking methods
• design integration; simulation and application of unique design methods for low power
Current Projects & Interest

- Circuit techniques and designs for low level high speed pipelining
- Clocking & synchronization issues in SIP
- Impact of interconnect behavior on clocking; synchronous & asynchronous circuits and their interface
- Embedded cores with special application to multimedia, communication & signal processing
• Power minimization
  – higher level power minimization
  – power modeling
  – delay modeling
• Hardware semantics to model a processor operations (at low level) to evaluate architectural features
JOBS

- Intel Corporation
- Sun Microsystems
- Sun Microelectronics
- Lockheed Martin
- IBM
- Allied Signals
- Motorola and more...
Ramalingam Sridhar

Email: rsridhar@cse.buffalo.edu
135 Bell Hall
“Everything that can be invented has been invented.”

(Charles Duell, Commissioner, U.S. Office of Patents, 1899)