1. 16 points
   a. Why do we gradually increase the size of the inverters in buffer design? Why not give the output of a circuit to one large inverter?
   b. Which is better? A 6 input NAND gate or the same redesigned with four 3 input NAND gates? Why?
   c. Consider the static CMOS gate shown in Fig. 1. Assume $V_{dd} = 2.5V$ and $V_{Th} = 0.5V$. Will the threshold voltages of the two NMOS transistors be the same? If yes, why? If not, why not?
   d. In CMOS, if we increase the load capacitance of an inverter, how does it affect the short circuit power (increase or decrease)? Why?

2. Consider the function $Y = A'BC + AB'C + ABC'$ 10 points
   a. Implement the above expression in compound CMOS logic style (PUN and PDN).
   b. Implement the above expression in Transmission logic style.

3. 10 points
   Calculate the noise margin below. ($V_{OL} = 0.5$, $V_{IL} = 3$, $V_{OH} = 4$, $V_{IH} = 3.8$)

4. 12 points
   a. Size for performance with equal rise and fall times
   b. Size for performance only
c. Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 6 and PMOS W/L = 10.

5. 12 points Briefly specify the three types of power consumption in CMOS technology. Give the factors that affect each of these (Hint: you may specify the equations in explaining).

6. 12 points Draw a rising edge triggered D flip-flop using Transmission gates. Explain how it functions.

7. 12 points Design a pass-transistor network that implements the following Boolean function:
   \[ D = A'B'C + AB'C + ABC' + (ABC)' \]

8. 16 points
   a. In order to drive a large capacitance \( C_L = 20 \text{ pF} \) from a minimum size gate (with input capacitance \( C_i = 10 \text{fF} \)), you decide to introduce a three-staged buffer. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the three additional buffer stages that will minimize the propagation delay. (\( N = 4 \) in total)

   b. If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?
   
   \( e = 2.718, \text{1pF} = 10^{-12}\text{F}, \text{1fF} = 10^{-15}\text{F} \)