1. The voltage transfer characteristics for an inverter are shown in Fig. 1. What are NML and NMH of the inverter?

Answer:
\[ V_{IL} = 1V, \quad V_{OL} = 0V, \quad \text{so NML} = 1V \]
\[ V_{IH} = 2V, \quad V_{OH} = 3V, \quad \text{so NMH} = 1V \]

2. Draw the transistor level schematic diagram of the CMOS gate that implements function Z:

a. \[ Z = \overline{A} \cdot B \cdot C + D + E' = ((A+B'+C').D'.E)' \]

b. \[ Z = (A \cdot B' \cdot C' + D)' \]

Assume that the Primary Inputs available are A, B, C, D and their complements.

A:
3. Consider the circuit in Fig. 2.
   (a) What is the logic function implemented by this circuit?
   (b) How would you implement this function with PMOS-only switches?
   Assume both true and complimentary input signals are available.

   Answer:
   \[ D = AB'C + ABC' + A'BC \]

   ![](image)

4. Assume inputs and its complements are available. If a Boolean function is \( D = A'BC + AB'C + AC' + B'C' \), then:
   (a) Implement the function using transmission gate and draw the transistor level schematic diagram.

   ![](image)
(b) Implement this function using a compound CMOS gate and draw the transistor level schematic diagram.

Answer:

A:

```
          B
         /A
         /B
          A
    /B         |         /C
     /C         C
    /C         /C
          /B
```

B:

```
A ——— /A ——— /A ——— /A ——— B
/ B ——— B ——— B ——— B
/ C ——— C ——— C ——— C

Vdd

A ——— /B ——— /C
/ A ——— A ——— A
/ C ——— C ——— C

Gnd
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