1. What function does the following CMOS circuit implement? What is (are) the shortest pull-up path and the shortest pull-down path?

Ans:

\[
out = (A + \overline{B} + \overline{C}) \cdot \overline{D} \cdot E + F
\]

shortest pull-up path: D'=F=0 or E=F=0
shortest pull-down path: F=1

b. Draw the circuit diagram of the Complementary Pass Transistor Logic circuit that
implements the function $F$, given by $F = ab + a'b'$

2. Sizing a chain of inverters.
   a. In order to drive a large capacitance ($C_L = 20$ pF) from a minimum size gate (with input capacitance $C_i = 10$ fF), you decide to introduce a two-staged buffer as shown in Figure below. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay (consider $\gamma = 1$).
   b. If we ignore self-loading effect, that is, $\gamma = 0$. If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?

'1' is the minimum size inverter.

Ans:

Minimum delay occurs when the delay through each buffer is the same. This can be achieved by sizing the buffer as $f, f_2$, respectively

Where

$$f = \sqrt[3]{N} \sqrt{F} = \sqrt[3]{\frac{2000}{20}} = 12.6$$
\[
\begin{align*}
    t_p &= N t_p^0 \left(1 + \frac{f}{f_g}\right) = 3 \cdot 70\text{ps} \cdot (1 + 12.6) = 2.8\text{ns}
\end{align*}
\]

From our lecture, we know that the minimum delay occurs when \( f = e \), therefore:

\[
    N = \frac{\ln(2000)}{\ln(f)} = 7.6
\]

Here you should calculate \( N = 7 \) and \( N = 8 \) both then get the final delay and choose between 7 and 8.

\[
    f = e^{\frac{\ln(2000)}{7}} = 2.96
\]

\[
    t_{delay} = 7 \times 3.96 \times 70\text{ps} = 1.9\text{ns}
\]

3. Transistor sizing: What is the logic function implemented by the static CMOS circuit shown below?

a. Size for performance with equal rise and fall times
   For sizing with equal rise and fall time we have to make sure that in each path the size of PMOS is 3 times the size of NMOS
   So for PMOS: A:6, B:6, C:3, D:3
   For NMOS: A:3, B:3, C:3, D:3

b. Size for performance only
   For PMOS: A:2, B:2, C:1, D:1
   For NMOS: A:3, B:3, C:3, D:3

c. Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 6 and PMOS W/L = 10.
   Ans:
   Looking into the circuit from the output node, the pull up network has the following three distinct paths to VDD: D=0, C=0, A=B=0. For each of these three paths, the resistance should be made equal to that of a PMOS of W/L=10. For transistors with input D and C,
setting their W/L=10 makes the output resistance of that path the same as the reference inverter. For the path A=B=0, setting the transistor sizes to each W/L=20 results in a resistance of R/2 in each of them (R is the resistance of the PMOS with W/L=10). This when A=B=0, the total resistance of that path would be R/2 + R/2 = R.

Now looking into the circuit from the output node, the pull down network has the following two distinct paths to ground: B=C=D=1, A=C=D=1. Using the idea described for the pull up network, the sizes for the pull down transistors can be computed as: NMOS transistors A, B, C and D are sized W/L = 18.

4. If the Boolean function of a complex gate is

\[ X = \left( \left( \left( A \land B \right) \lor C \right) \land \left( D \land E \land F \right) \right) \land (G \land H \lor I) \]

a) Please show the schematic of the CMOS complex gate in terms of PMOS and NMOS ONLY.
   Ans:

   ![CMOS complex gate schematic]

b) If the output of the above complex full-static gate is driving a load of \( C_L \), we use \( R_n \) and \( R_p \) to denote the channel resistance of a unit NMOS and a unit PMOS (W/L = 2um/1um), respectively. What will be the worst-case rising and falling delay? In your computation, assume that all NMOS and PMOS transistors are unit transistors (W/L = 2um/1um), and the internal capacitances can be ignored.
   Ans:
   In the worse case,
   The rising delay is \( T_r = 3R_p * C_L \)
   The falling delay is \( T_f = 5R_n * C_L \)