1. Transitional probability: For the circuit shown in figure 1, derive the transitional probability $P_{0\rightarrow1}$, given $P_A = 0.3$, $P_B = 0.5$, $P_C = 0.8$, $P_D = 0.4$. $P_A$, $P_B$, $P_C$ and $P_D$ indicate the probabilities that A, B, C and D are 1 respectively.

![Fig 1.](image)

**OR gate:**

$P(0) = (1-P_A)(1-P_B) = 0.7*0.5 = 0.35$

$P(1) = 1 - P(0) = 0.65$

**AND gate:**

$P(1) = P_C * P_D = 0.8*0.4 = 0.32$

$P(0) = 0.68$

**XOR gate:**

$P(0 \rightarrow 1) = P(0) * P(1) = (\text{AND}(0)*\text{OR}(0) + \text{AND}(1)*\text{OR}(1)) * (1-(\text{AND}(0)*\text{OR}(0) + \text{AND}(1)*\text{OR}(1)))$

$= (0.68*0.35 + 0.32*0.65 ) * (1-(0.68*0.35 + 0.32*0.65 ) )$

$= 0.446*0.554 = 0.247$

2. For the schematic shown below, identify the function $F$ implemented in the circuit, and draw the transistor-level circuit diagram for $F$ using the logic styles – Static CMOS and Dynamic CMOS.
3. Implement $F = ABC + ACD$ (and $\overline{F}$) in DCVSL. Assume A, B, C, D, and their complements are available as inputs.
4. Dynamic circuits: Consider the domino stage shown below. Assume that each of the PDN in the figure has a single NMOS transistor. Assume the precharge time, evaluate time, propagation delay of the static inverter are all equal to 10ns each. Also assume zero rise and fall times for all signals. Complete the timing diagram for signals Out1, Out2, Out3 and Out4 if the IN signal goes high at the rising edge of the clock. Assume clock period is 100ns.

Ans: