Resource Limited Inference in SNePS

a project for cs642 fall, 1981

by Gerard Donlon
1. Introduction

I have implemented resource limited inference in SNePS. With my additions to SNePS, a user can specify "how hard" the system can work on one inference. When the specified amount of work has been done, the inference stops and returns only those answers that were found. There may or may not be more answers to find when the system reaches a resource limit. If there are more answers and the user restarts the inference with more resources, the new answers will be found.

Reaching a resource limit is transparent to the user. That is, answers are returned in exactly the same way when inference has been exhausted as when a resource bound is encountered.

2. Overview of the System

SNIPS is implemented using MULTI, a multiprocessing package for LISP. Inference is done by starting a set of processes that will produce the required results. Each process is a non-interuptable function that may create or initiate any number of processes. Answers produced by processes are retained so that future inferences may use these answers without re-doing the inference. This will create a graph of processes.

Some of these processes control the order of execution of other processes or group processes into sets of related processes. These processes are called monitors.

The resource that will be limited is network matches. That choice was made because the number of matches done is easy to
count and is the slowest operation in the inference system.

Monitors are the obvious place to control the amount of resources a set of processes may use. To implement this, I added two registers to each process. Register \texttt{RMAX}: is the maximum number of resources a process may consume. Register \texttt{RSOURCE}: contains a list of monitors that will contribute resources to the process and the number of resources the monitor is willing to contribute. When a process is ready to execute, it first checks to see if it is possible to finish using \texttt{RMAX}: or less resources. If it is possible, the process then checks to make sure its sources really have the resources to contribute. This two-step process of resource allocation allows a monitor to initially give all of its resources to each process it initiates. When these processes execute, some may use resources. When they do, they decrement the monitor's total. If a process tries to execute when the monitor's total is too small, the process suspends itself.

If two or more processes with different sources initiate a process, that process's \texttt{RMAX}: will be the sum of the maximum allowed by each initiating process. And that process's \texttt{RSOURCE}: will be the union of the sources of the initiating processes. That way, processes that produce answers that are important to several processes will receive larger resource counts.

The two-step allocation procedure forces the scheduler to determine which processes will get the resources. And, since the process will not use more than \texttt{RMAX}: resources units, the monitor can also limit the number of resources available to any
process. By not forcing the monitor to allocate its resources statically, the monitor can maintain a pool of resources that can be allocated to any process below the monitor that needs them. It also prevents wasting resources since any process that does not use resources will not take them, even if the monitor allows it.

A special case of resource allocation allows an infinite number of resources. This is the default when the user does not specify a limit.

Limiting resources has an interesting effect on the non-derivable monitor. That monitor tries to deduce some consequent or its negation. If it can not, it reports that its argument is not derivable in the current network. If the monitor stops with no answer and some process below it was suspended because of a resource bound, the consequent may be derivable in the network but not in the resource bound given. So, instead of being non-derivable, the consequent is "not obvious". Since this may not be what the user wants, there is a special resource limit for non-derivable monitors. By default, every non-derivable monitor is allowed an infinite number of resource units. If anyone wants to, they can change that limit to be anything, including the standard allocation procedure, by changing the variable I-MTRLIMITS. The passing of resource limits is done by the functions NEW and INITIATE. The default for NEW is no resources passed. The default for INITIATE is the RMAX: and RSOURCE: of the initiateing process. When using all of the defaults, the system behaves exactly as it did before adding resource limits.
3. Applications

Resource limited inference may be used to set up a context in which all further inference will be performed. [Martins] shows how this can solve the symbol mapping problem and reduces the problems caused by fan out in full forward or backward inference. The technique has been called bi-directional inference.

A second application, mentioned earlier, is changing the nonderivable operator into a "not obvious" operator. With a resource limit of 1 placed on the nonderivable monitor, $\forall(x)\text{BIRD}(x) \Rightarrow \Delta \text{FLIES}(x)$ means that if $x$ is a bird and it is not asserted in the network that $x$ does not fly, then assume $x$ flies. By changing the resource limit on the nonderivable monitor, you change the interpretation of "obvious".

A third application is resource-slicing through a deduction. It is similar to time-slicing but you limit the number of resources used, not time used. For instance, if we have $\forall_I^1(a, b, c, d)$ and $c$ is easy to prove and $a, b$ and $d$ are not easy to prove, then by setting up a resource slicing monitor, we can prove $\neg a, \neg b, \neg d$ and $c$ in four times the minimum number of resources required. A random order can take some fraction of the maximum.

4. Status

Resource limited inference has been added to SNePS and it is working. A user can specify a resource bound on any ADD, DEDUCE or RESUME by including the symbol $<$ followed by an integer or
INF. INF is the default.

The nonderivable monitor limits can be set by setting the variable I-//-MTRLIMITS to any function. When evaled, the value returned should be a list whose first element will be RMAX: and whose second element will be RESOURCE:. By default, I-//-MTRLIMITS is "'(INF NIL) which allows infinite resources without charging any monitor.

I have started implementing resource-slicing in the verify andor process. This work is not complete.

5. Future Work

1. Finish resource-slicing in VANDOR and similar processes.

2. Write a guide to the number of resources needed by an inferance. This should be investigated. It seems that to do L levels of inferance, you need (FAN-OUT-OF-RULES)\(^L\) resource units but I have not shown that.

3. The scheduler could be changed to run process with the largest resource count first. That would change the guide to the number of resources needed since that formula depends on a first in first out scheduler.

4. heuristics could be added to resource-slicing monitors to guide them to the easiest answer.

5. You could consider measuring some resource other than network matches.
An example of a run with resource limited inference.

The rules assert that all elephants are grey. All subs are grey. And, anything that is grey is a sub. By adding a resource bound, I prevent the last rule from being used.

ALISP VERSION 3.3 22 DECEMBER 1981 4:09 PM

$ ? (LOAD '(SNEPS CSDTEMP))
SNEPS

********** SYSTEM NOT TESTED YET. **********************
PATH BASED INFERENCE HAS BEEN ADDED TO SNEPS.

(SNEPS INITIALIZED FOR BATCH OPERATION COMPILED 81 10 28)

$ ? (LENGTH (INPUT (SNEPSRC CSDLIB)(SNEPSREAD SNEPSREAD1 NUMB?))))

3
$ ? (LENGTH (INPUT (TEMP CSDXGFD))))))
6
$ ? (LENGTH (INPUT (AINF CSDXGFD))))))
131
$ ? (EV-TRACE)
T
$ ? (SNEPS)

SNEPS

$* (DEFINE MEM MEM- CLASS CLASS- COLOROF COLOROF- IS IS-)
(MEM MEM-)
(CLASS CLASS-)
(COLOROF COLOROF-)
(IS IS-)
(DEFINED)
11 MSEC

$* (BUILD AVB $X
$* ANT (BUILD MEM *X CLASS ELEPHANT)
$* CQ (BUILD COLOROF *X IS GREY))
(M3)
33 MSEC

$* (BUILD AVB $X
$* ANT (BUILD MEM *X CLASS SUBS)
$* CQ (BUILD COLOROF *X IS GREY))
(M6)
32 MSEC

$* (BUILD AVB $X
$* ANT (BUILD COLOROF *X IS GREY)
$* CQ (BUILD MEM *X CLASS SUBS))
(M9)
32 MSECS

$* (ADD MEM CLYDE CLASS ELEPHANT < 1)

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX:1
RSOURCE: NIL

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX:1
RSOURCE: ((P61 1))

***** "ENTERING" PROCESS : P60 *****
NAME: F-INFER
CLINK: NIL
NODE : M10
RMAX:1
RSOURCE: ((P61 1))

***** "LEAVING" PROCESS : P60 *****
NAME: F-INFER
CLINK: NIL
NODE: M10
RMAX:0
RSOURCE: ((P61 0))

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX:0
RSOURCE: ((P61 1))

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX:0
RSOURCE: ((P61 1))

***** "ENTERING" PROCESS : P66 *****
NAME: GO-UP
CLINK: P62
CQ: M3
BNDG: ((V1, CLYDE))
RMAX:0
SOURCE: NIL

***** "LEAVING" PROCESS: P66 *****
NAME: GO-UP
CLINK: P62
CQ: M3
BNDG: ((V1, CLYDE))
RMAX: 0
RSOURCE: NIL

***** "ENTERING" PROCESS: P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE: (P60)
EVENTS: NIL
RMAX: 0
RSOURCE: ((P61))

***** "LEAVING" PROCESS: P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE: (P60)
EVENTS: NIL
RMAX: 0
RSOURCE: ((P61))

***** "ENTERING" PROCESS: P68 *****
NAME: USE
CLINK: P67
BOSSES: ((P67, M2))
CQ: (M2)
RULE: M3
BNDG: ((V1, CLYDE))
MSG: NIL
RMAX: 0
RSOURCE: NIL

***** "LEAVING" PROCESS: P68 *****
NAME: USE
CLINK: P67
BOSSES: ((P67, M2))
CQ: (M2)
RULE: M3
BNDG: ((V1, CLYDE))
MSG: NIL
RMAX: 0
RSOURCE: NIL

***** "ENTERING" PROCESS: P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE: (P60)
EVENTS: NIL
RMAX: 0
RSOURCE: ((P61))

***** "LEAVING" PROCESS: P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: 0
RSOURCE: ((P61 1))

***** "ENTERING" PROCESS : P69 *****
NAME: CHENT
CLINK: P67
BOSSES: ((P67,M2))
CQ: (M2)
ANT: (M1)
BNOG: ((V1,CLYDE))
MSG: NIL
RMAX: 0
RSOURCE: NIL

***** "LEAVING" PROCESS : P69 *****
NAME: CHENT-R
CLINK: P67
BOSSES: ((P67,M2))
CQ: (M2)
ANT: (M1)
BNOG: ((V1,CLYDE))
MSG: ((M1 (M10 ((V1,CLYDE)))))
RMAX: 0
RSOURCE: NIL

***** "ENTERING" PROCESS : P69 *****
NAME: CHENT-R
CLINK: P67
BOSSES: ((P67,M2))
CQ: (M2)
ANT: (M1)
BNOG: ((V1,CLYDE))
MSG: ((M1 (M10 ((V1,CLYDE)))))
RMAX: 0
RSOURCE: NIL

SINCE
(M1 (CLASS (ELEPHANT)) (MEM (V1 (:VAR (T)) (:VAL (CLYDE)))))
WE INFER
(M2 (IS (GREY)) (COLOROF (V1 (:VAR (T)) (:VAL (CLYDE)))))

***** "LEAVING" PROCESS : P69 *****
NAME: CHENT-R
CLINK: P67
BOSSES: ((P67,M2))
CQ: (M2)
ANT: (M1)
BNOG: ((V1,CLYDE))
MSG: NIL
RMAX: 0
RSOURCE: NIL
***** "ENTERING" PROCESS : P67 *****
NAME: ANS-CATCH
CLINK: P62
BOSSES: (P62)
DATA: NIL
MSG: (((M2 ((V1,CLYDE)))))
RMAX: 0
RSOURCE: NIL

***** "LEAVING" PROCESS : P67 *****
NAME: ANS-CATCH
CLINK: P62
BOSSES: (P62)
DATA: (((M2 ((V1,CLYDE))))
MSG: NIL
RMAX: 0
RSOURCE: NIL

***** "ENTERING" PROCESS : P62 *****
NAME: IMPLY
CLINK: NIL
BOSSES: NIL
CQ: (M2)
RULE: M3
BNDG: ((V1,CLYDE))
MSG: (((M2 ((V1,CLYDE))))
RMAX: 0
RSOURCE: NIL

***** "LEAVING" PROCESS : P62 *****
NAME: IMPLY
CLINK: NIL
BOSSES: ((P70,M2))
CQ: (M2)
RULE: M3
BNDG: ((V1,CLYDE))
MSG: NIL
RMAX: 0
RSOURCE: NIL

***** "ENTERING" PROCESS : P70 *****
NAME: ANS-CATCH
CLINK: NIL
BOSSES: NIL
DATA: NIL
MSG: (((M2 ((V1,CLYDE))))
RMAX: 0
RSOURCE: NIL

***** "LEAVING" PROCESS : P70 *****
NAME: ANS-CATCH
CLINK: NIL
BOSSES: NIL
DATA: (((M2 ((V1,CLYDE))))
MSG: NIL
RMAX: 0
RSOURCE: NIL
***** "ENTERING" PROCESS: P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE: (P60)
EVENTS: NIL
RMAX: 0
RSOURCE: ((P61 1))

***** "LEAVING" PROCESS: P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE: (P60)
EVENTS: NIL
RMAX: 0
RSOURCE: ((P61 1))

***** "ENTERING" PROCESS: P63 *****
NAME: I-MTR
CLINK: NIL
QUEUE: NIL
EXTRAS: NIL
RMAX: 0
RSOURCE: NIL

***** "LEAVING" PROCESS: P63 *****
NAME: I-MTR
CLINK: NIL
QUEUE: NIL
EXTRAS: NIL
RMAX: 0
RSOURCE: NIL

***** "ENTERING" PROCESS: P71 *****
NAME: F-INFER
CLINK: NIL
NODE: M11
RMAX: 0
RSOURCE: NIL

***** "LEAVING" PROCESS: P71 *****
NAME: F-INFER
CLINK: NIL
NODE: M11
RMAX: 0
RSOURCE: NIL

***** "ENTERING" PROCESS: P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE: (P60)
EVENTS: NIL
RMAX: 0
RSOURCE: ((P61 1))

SUSPENDING P61
APPENDIX 1

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: 0
RSOURCE: ((P61 1))

(M10 M11)
1687 MSECS

$* (DEDUCE COLOROF CLYDE IS GREY)

***** "ENTERING" PROCESS : P74 *****
NAME: I-MTR
CLINK: NIL
QUEUE (P73)
EXTRAS NIL
RMAX: INF
RSOURCE: ((P74 INF))

***** "LEAVING" PROCESS : P74 *****
NAME: I-MTR-R
CLINK: NIL
QUEUE NIL
EXTRAS NIL
RMAX: INF
RSOURCE: ((P74 INF))

***** "ENTERING" PROCESS : P73 *****
NAME: INFER
CLINK: P75
CQ: T72
BNDG: NIL
MSG: NIL
RMAX: INF
RSOURCE: ((P74 INF))

WE KNOW
(T72 (IS (GREY)) (COLOROF (CLYDE)))

***** "LEAVING" PROCESS : P73 *****
NAME: INFER
CLINK: P75
CQ: T72
BNDG: NIL
MSG: NIL
RMAX: INF
RSOURCE: ((P74 INF))

***** "ENTERING" PROCESS : P75 *****
NAME: TOPMOST-TOPINF
CLINK: NIL
CQ: T72
DATA: NIL
MSG: ((T72 (M11 NIL)))
N-ANS: 0
P-ANS: 0
TOT: NIL
N-POS: NIL
N-NEG: NIL
*SUSPS* NIL
BOSSES: NIL
MTR: P74
RMAX: INF
RSOURCE: ((P74 INF) (P74 INF))

***** "LEAVING" PROCESS : P75 *****
NAME: TOPMOST-TOPINF
CLINK: NIL
CQ: T72
DATA: ((M11 NIL))
MSG: NIL
N-ANS: 0
P-ANS: 1
TOT: NIL
N-POS: NIL
N-NEG: NIL
#SUSPS# NIL
BOSSES: NIL
MTR: P74
RMAX: INF
RSOURCE: ((P74 INF) (P74 INF))

***** "ENTERING" PROCESS : P74 *****
NAME: I-MTR-R
CLINK: NIL
QUEUE NIL
EXTRAS NIL
RMAX: INF
RSOURCE: ((P74 INF))

***** "LEAVING" PROCESS : P74 *****
NAME: I-MTR
CLINK: NIL
QUEUE NIL
EXTRAS NIL
RMAX: INF
RSOURCE: ((P74 INF))

(M11)
401 Msecs

$* (DESCRIBE *NODES)
(M11 (IS (GREY)) (COLOROF (CLYDE)))
(CLYDE)
(M10 (CLASS (ELEPHANT)) (MEM (CLYDE)))
(M9 (CQ (M8 (CLASS (SUBS)) (MEM (V3 (:VAR (T))))))
  (ANT (M7 (IS (GREY)) (COLOROF (V3 (:VAR (T))))))
  (AVB (V3 (:VAR (T)))))
(M8 (CLASS (SUBS)) (MEM (V3 (:VAR (T))))
(M7 (IS (GREY)) (COLOROF (V3 (:VAR (T)))))
(V3 (:VAR (T)))
(M6 (CQ (M5 (IS (GREY)) (COLOROF (V2 (:VAR (T))))))
   (ANT (M4 (CLASS (SUBS)) (MEM (V2 (:VAR (T))))))
   (AVB (V2 (:VAR (T)))))
(M5 (IS (GREY)) (COLOROF (V2 (:VAR (T))))
(SUBS)
(M4 (CLASS (SUBS)) (MEM (V2 (:VAR (T))))
(V2 (:VAR (T))))
(M3 (CQ (M2 (IS (GREY)) (COLOROF (V1 (:VAR (T)) (:VAL (CLYDE))))))
   (ANT (M1 (CLASS (ELEPHANT)) (MEM (V1 (:VAR (T)) (:VAL
(CLYDE))))))
   (AVB (V1 (:VAR (T)) (:VAL (CLYDE))))
(GREY)
(M2 (IS (GREY)) (COLOROF (V1 (:VAR (T)) (:VAL (CLYDE))))
(ELEPHANT)
(M1 (CLASS (ELEPHANT)) (MEM (V1 (:VAR (T)) (:VAL (CLYDE))))
(V1 (:VAR (T)) (:VAL (CLYDE))))
(X (:VAL (V3 (:VAR (T))))
(DUMPED)
320 MSECS

$* (LISP)
END SNEPS
$ ? (EXIT)
END ALISP RUN
7. APPENDIX 2

This run has the same data as the previous run, but gives an infinite number of resources to the add. Notice that it asserts that Clyde is a sub.

ALISP VERSION 3.3  22 DECEMBER 1981  9:54 PM

$ ? (LOAD '(SNEPS CSDTEMP))
SNEPS  UDM4.0.1

********** SYSTEM NOT TESTED YET. ********************
PATH BASED INFERANCE HAS BEEN ADDED TO SNEPS.

(SNEPS INITIALIZED FOR BATCH OPERATION  COMPILED 81 10 28)
$ ? (LENGTH (INPUT (SNEPSRC CSDLIB)(SNEPSREAD SNEPSREAD1 NUMB?))))

3
$ ? (LENGTH (INPUT (TEMP CSDXGFD))))))
6
$ ? (LENGTH (INPUT (AINF CSDXGFD)))))))))
131
$ ? (EV-TRACE)
T
$ ? (SNEPS)
SNEPS
$* (DEFINE MEM MEM- CLASS CLASS- COLOROF COLOROF- IS IS-)
  (MEM MEM-)
  (CLASS CLASS-)
  (COLOROF COLOROF-)
  (IS IS-)
  (DEFINED)
  11 MSEC

$* (BUILD AVB $X
$*        ANT (BUILD MEM *X CLASS ELEPHANT)
$*        CQ (BUILD COLOROF *X IS GREY))
  (M3)
  34 MSEC

$* (BUILD AVB $X
$*        ANT (BUILD MEM *X CLASS SUBS)
$*        CQ (BUILD COLOROF *X IS GREY))
  (M6)
  35 MSEC

$* (BUILD AVB $X
$*        ANT (BUILD COLOROF *X IS GREY)
$*        CQ (BUILD MEM *X CLASS SUBS))
  (M9)
  35 MSEC

$* (ADD MEM CLYDE CLASS ELEPHANT < INF)

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: NIL

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P60 *****
NAME: F-INFER
CLINK: NIL
NODE: M10
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P60 *****
NAME: F-INFER
CLINK: NIL
NODE: M10
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P66 *****
NAME: GO-UP
CLINK: P62
CQ: M3
BNDG: ((V1, CLYDE))
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P66 *****
NAME: GO-UP
CLINK: P62
CQ: M3
BNDG: ((V1, CLYDE))
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P68 *****
NAME: USE
CLINK: P67
BOSSES: ((P67, M2))
CQ: (M2)
RULE: M3
BNDG: ((V1, CLYDE))
MSG: NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P68 *****
NAME: USE
CLINK: P67
BOSSES: ((P67, M2))
CQ: (M2)
RULE: M3
BNDG: ((V1, CLYDE))
MSG: NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))
***** "ENTERING" PROCESS : P69 *****
NAME: CHENT
CLINK: P67
BOSSES: ((P67,M2))
CQ: (M2)
ANT: (M1)
BNDG: ((V1,CLYDE))
MSG: NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P69 *****
NAME: CHENT-R
CLINK: P67
BOSSES: ((P67,M2))
CQ: (M2)
ANT: (M1)
BNDG: ((V1,CLYDE))
MSG: ((M1 (M10 ((V1,CLYDE)))))
RMAX:INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P69 *****
NAME: CHENT-R
CLINK: P67
BOSSES: ((P67,M2))
CQ: (M2)
ANT: (M1)
BNDG: ((V1,CLYDE))
MSG: ((M1 (M10 ((V1,CLYDE)))))
RMAX:INF
RSOURCE: ((P61 INF))

SINCE
(M1 (CLASS (ELEPHANT)) (MEM (V1 (:VAR (T)) (:VAL (CLYDE)))))

WE INFERENCE
(M2 (IS (GREY)) (COLOROF (V1 (:VAR (T)) (:VAL (CLYDE))))))

***** "LEAVING" PROCESS : P69 *****
NAME: CHENT-R
CLINK: P67
BOSSES: ((P67,M2))
CQ: (M2)
ANT: (M1)
BNDG: ((V1,CLYDE))
MSG: NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P67 *****
NAME: ANS-CATCH
CLINK: P62
BOSSES: (P62)
DATA: NIL
MSG: (((M2 ((V1,CLYDE))))
RMAX:INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P67 *****
NAME: ANS-CATCH
CLINK: P62
BOSSES: (P62)
DATA: ((M2 ((V1,CLYDE))))
MSG: NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P62 *****
NAME: IMPLY
CLINK: NIL
BOSSES: NIL
CQ: (M2)
RULE: M3
BNDG: ((V1,CLYDE))
MSG: (M2 ((V1,CLYDE)))))
RMAX:INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P62 *****
NAME: IMPLY
CLINK: NIL
BOSSES: ((P70,M2))
CQ: (M2)
RULE: M3
BNDG: (V1,CLYDE))
MSG: NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P70 *****
NAME: ANS-CATCH
CLINK: NIL
BOSSES: NIL
DATA: NIL
MSG: (M2 ((V1,CLYDE))))
RMAX:INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P70 *****
NAME: ANS-CATCH
CLINK: NIL
BOSSES: NIL
DATA: (M2 ((V1,CLYDE))))
MSG: NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
***** "LEAVING" PROCESS: P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS: P63 *****
NAME: I-MTR
CLINK: NIL
QUEUE NIL
EXTRAS NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS: P63 *****
NAME: I-MTR
CLINK: NIL
QUEUE NIL
EXTRAS NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS: P71 *****
NAME: F-INFER
CLINK: NIL
NODE: M11
RMAX:INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS: P71 *****
NAME: F-INFER
CLINK: NIL
NODE: M11
RMAX:INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS: P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS: P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX:INF
RSOURCE: ((P61 INF))
***** "ENTERING" PROCESS : P76 *****
NAME: GO-UP
CLINK: P72
CQ: M9
BNDG: ((V3,CLYDE))
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P76 *****
NAME: GO-UP
CLINK: P72
CQ: M9
BNDG: ((V3,CLYDE))
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P78 *****
NAME: USE
CLINK: P77
BOSSES: ((P77,M8))
CQ: (M8)
RULE: M9
BNDG: ((V3,CLYDE))
MSG: NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P78 *****
NAME: USE
CLINK: P77
BOSSES: ((P77,M8))
CQ: (M8)
RULE: M9
BNDG: ((V3,CLYDE))
MSG: NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
**APPENDIX 2**

QUEUE (P60)
EVENTS NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P79 *****
NAME: CHENT
CLINK: P77
BOSSES: ((P77,M8))
CQ: (M8)
ANT: (M7)
BNDG: ((V3,CLYDE))
MSG: NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P79 *****
NAME: CHENT-R
CLINK: P77
BOSSES: ((P77,M8))
CQ: (M8)
ANT: (M7)
BNDG: ((V3,CLYDE))
MSG: ((M7 (M11 ((V3,CLYDE)))))
RMAX:INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P79 *****
NAME: CHENT-R
CLINK: P77
BOSSES: ((P77,M8))
CQ: (M8)
ANT: (M7)
BNDG: ((V3,CLYDE))
MSG: ((M7 (M11 ((V3,CLYDE)))))
RMAX:INF
RSOURCE: ((P61 INF))

SINCE
(M7 (IS (GREY)) (COLOROF (V3 (:VAR (T)) (:VAL (CLYDE))))))

WE INFER
(M8 (CLASS (SUBS)) (MEM (V3 (:VAR (T)) (:VAL (CLYDE))))))

***** "LEAVING" PROCESS : P79 *****
NAME: CHENT-R
CLINK: P77
BOSSES: ((P77,M8))
CQ: (M8)
APPENDIX 2

ANT: (M7)
BNDG: ((V3, CLYDE))
MSG: NIL
RMAX: INF
RSOURC: ((P61 INF))

***** "ENTERING" PROCESS : P77 *****
NAME: ANS-CATCH
CLINK: P72
BOSSES: (P72)
DATA: NIL
MSG: (((M8 ((V3, CLYDE))))
RMAX: INF
RSOURC: ((P61 INF))

***** "LEAVING" PROCESS : P77 *****
NAME: ANS-CATCH
CLINK: P72
BOSSES: (P72)
DATA: (((M8 ((V3, CLYDE))))
MSG: NIL
RMAX: INF
RSOURC: ((P61 INF))

***** "ENTERING" PROCESS : P72 *****
NAME: IMPLY
CLINK: NIL
BOSSES: NIL
CQ: (M8)
RULE: M9
BNDG: ((V3, CLYDE))
MSG: (((M8 ((V3, CLYDE))))
RMAX: INF
RSOURC: ((P61 INF))

***** "LEAVING" PROCESS : P72 *****
NAME: IMPLY
CLINK: NIL
BOSSES: ((P80, M8))
CQ: (M8)
RULE: M9
BNDG: ((V3, CLYDE))
MSG: NIL
RMAX: INF
RSOURC: ((P61 INF))

***** "ENTERING" PROCESS : P80 *****
NAME: ANS-CATCH
CLINK: NIL
BOSSES: NIL
DATA: NIL
MSG: (((M8 ((V3, CLYDE))))
RMAX: INF
RSOURC: ((P61 INF))

***** "LEAVING" PROCESS : P80 *****
NAME: ANS-CATCH
APPENDIX 2

CLINK: NIL
BOSSES: NIL
DATA: ((M8 ((V3, CLYDE))))
MSG: NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P73 *****
NAME: I-MTR
CLINK: NIL
QUEUE NIL
EXTRAS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P73 *****
NAME: I-MTR
CLINK: NIL
QUEUE NIL
EXTRAS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P81 *****
NAME: F-INFER
CLINK: NIL
NODE: M12
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P81 *****
NAME: F-INFER
CLINK: NIL
NODE: M12
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: GO-UP
CLINK: P82
CQ: M6
BNDG: ((V2, CLYDE))
RMAX:INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: USE
CLINK: P87
BOSSES: ((P87, M5))
CQ: (M5)
RULE: M6
BNDG: ((V2, CLYDE))
MSG: NIL
RMAX:INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P68 *****
NAME: USE
APPENDIX 2

CLINK: P87
BOSSES: ((P87,M5))
CQ: (M5)
RULE: M6
BNDG: ((V2,CLYDE))
MSG: NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P89 *****
NAME: CHENT
CLINK: P87
BOSSES: ((P87,M5))
CQ: (M5)
ANT: (M4)
BNDG: ((V2,CLYDE))
MSG: NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P89 *****
NAME: CHENT-R
CLINK: P87
BOSSES: ((P87,M5))
CQ: (M5)
ANT: (M4)
BNDG: ((V2,CLYDE))
MSG: ((M4 (M12 ((V2,CLYDE)))))
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P89 *****
NAME: CHENT-R
CLINK: P87
BOSSES: ((P87,M5))
CQ: (M5)
ANT: (M4)
BNDG: ((V2,CLYDE))
MSG: ((M4 (M12 ((V2,CLYDE))))
RMAX: INF
RSOURCE: ((P61 INF))
APPENDIX 2

SINCE
(M4 (CLASS (SUBS)) (MEM (V2 (:VAR (T)) (:VAL (CLYDE)))))

WE INFER
(M5 (IS (GREY)) (COLOROF (V2 (:VAR (T)) (:VAL (CLYDE)))))

***** "LEAVING" PROCESS : P89 *****
NAME: CHENT-R
CLINK: P87
BOSSES: ((P87,M5))
CQ: (M5)
ANT: (M4)
BNDG: ((V2,CLYDE))
MSG: NIL
RMAX: INF
RSOURCE: ( (P61 INF))

***** "ENTERING" PROCESS : P87 *****
NAME: ANS-CATCH
CLINK: P82
BOSSES: (P82)
DATA: NIL
MSG: (((M5 ((V2,CLYDE))))
RMAX: INF
RSOURCE: ( (P61 INF))

***** "LEAVING" PROCESS : P87 *****
NAME: ANS-CATCH
CLINK: P82
BOSSES: (P82)
DATA: (((M5 ((V2,CLYDE))))
MSG: NIL
RMAX: INF
RSOURCE: ( (P61 INF))

***** "ENTERING" PROCESS : P82 *****
NAME: IMPLY
CLINK: NIL
BOSSES: NIL
CQ: (M5)
RULE: M6
BNDG: ((V2,CLYDE))
MSG: (((M5 ((V2,CLYDE))))
RMAX: INF
RSOURCE: ( (P61 INF))

***** "LEAVING" PROCESS : P82 *****
NAME: IMPLY
CLINK: NIL
BOSSES: ((P90,M5))
CQ: (M5)
RULE: M6
BNDG: ((V2,CLYDE))
MSG: NIL
RMAX: INF
RSOURCE: ( (P61 INF))
***** "ENTERING" PROCESS : P90 *****
NAME: ANS-CATCH
CLINK: NIL
BOSSES: NIL
DATA: NIL
MSG: ((M5 ((V2,CLYDE)))))
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P90 *****
NAME: ANS-CATCH
CLINK: NIL
BOSSES: NIL
DATA: ((M5 ((V2,CLYDE)))))
MSG: NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P83 *****
NAME: I-MTR
CLINK: NIL
QUEUE NIL
EXTRAS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "LEAVING" PROCESS : P83 *****
NAME: I-MTR
CLINK: NIL
QUEUE NIL
EXTRAS NIL
RMAX: INF
RSOURCE: ((P61 INF))

***** "ENTERING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX: INF
RSOURCE: ((P61 INF))

SUSPENDING P61

***** "LEAVING" PROCESS : P61 *****
NAME: RES-MTR-R
CLINK: NIL
QUEUE (P60)
EVENTS NIL
RMAX:INF
RSOURCE: ((P61 INF))

(M10 M11 M12)
4474 MSECS

$* (DEDUCE COLOROF CLYDE IS GREY)

***** "ENTERING" PROCESS : P93 *****
NAME: I-MTR
CLINK: NIL
QUEUE (P92)
EXTRAS NIL
RMAX:INF
RSOURCE: ((P93 INF))

***** "LEAVING" PROCESS : P93 *****
NAME: I-MTR-R
CLINK: NIL
QUEUE NIL
EXTRAS NIL
RMAX:INF
RSOURCE: ((P93 INF))

***** "ENTERING" PROCESS : P92 *****
NAME: INFER
CLINK: P94
CQ: T91
BNDG: NIL
MSG: NIL
RMAX:INF
RSOURCE: ((P93 INF))

WE KNOW
(T91 (IS (GREY)) (COLOROF (CLYDE)))

***** "LEAVING" PROCESS : P92 *****
NAME: INFER
CLINK: P94
CQ: T91
BNDG: NIL
MSG: NIL
RMAX:INF
RSOURCE: ((P93 INF))

***** "ENTERING" PROCESS : P94 *****
NAME: TOPMOST-TOFINF
CLINK: NIL
CQ: T91
DATA: NIL
MSG: ((T91 (M11 NIL)))
N-ANS: 0
P-ANS: 0
TOT: NIL
N-POS: NIL
N-NEG: NIL
#SUSPS# NIL
BOSSES: NIL
MTR: P93
RMAX: INF
RSOURCE: ((P93 INF) (P93 INF))

***** "LEAVING" PROCESS : P94 *****
NAME: TOPMOST-TOPINF
CLINK: NIL
CQ: T91
DATA: ((M11 NIL))
MSG: NIL
N-ANS: 0
P-ANS: 1
TOT: NIL
N-POS: NIL
N-NEG: NIL
#SUSPS# NIL
BOSSES: NIL
MTR: P93
RMAX: INF
RSOURCE: ((P93 INF) (P93 INF))

***** "ENTERING" PROCESS : P93 *****
NAME: I-MTR-R
CLINK: NIL
QUEUE NIL
EXTRAS NIL
RMAX: INF
RSOURCE: ((P93 INF))

***** "LEAVING" PROCESS : P93 *****
NAME: I-MTR
CLINK: NIL
QUEUE NIL
EXTRAS NIL
RMAX: INF
RSOURCE: ((P93 INF))

(M11)
411 MSECS

$* (DESCRIBE *NODES)
(M12 (CLASS (SUBS)) (MEM (CLYDE)))
(M11 (IS (GREY)) (COLOROF (CLYDE)))
(CLYDE)
(M10 (CLASS (ELEPHANT)) (MEM (CLYDE)))
(M9 (CQ (M8 (CLASS (SUBS))) (MEM (V3 (:VAR (T)) (:VAL (CLYDE))))))

(ANT (M7 (IS (GREY))) (COLOROF (V3 (:VAR (T)) (:VAL (CLYDE))))))

(AVB (V3 (:VAR (T)) (:VAL (CLYDE))))

(M8 (CLASS (SUBS))) (MEM (V3 (:VAR (T)) (:VAL (CLYDE))))

(M7 (IS (GREY))) (COLOROF (V3 (:VAR (T)) (:VAL (CLYDE))))

(V3 (:VAR (T)) (:VAL (CLYDE))))

(M6 (CQ (M5 (IS (GREY))) (COLOROF (V2 (:VAR (T)) (:VAL (CLYDE))))))

(ANT (M4 (CLASS (SUBS))) (MEM (V2 (:VAR (T)) (:VAL (CLYDE))))))

(AVB (V2 (:VAR (T)) (:VAL (CLYDE))))

(M5 (IS (GREY))) (COLOROF (V2 (:VAR (T)) (:VAL (CLYDE))))

(SUBS)

(M4 (CLASS (SUBS))) (MEM (V2 (:VAR (T)) (:VAL (CLYDE))))

(V2 (:VAR (T)) (:VAL (CLYDE))))

(M3 (CQ (M2 (IS (GREY))) (COLOROF (V1 (:VAR (T)) (:VAL (CLYDE))))))

(ANT (M1 (CLASS (ELEPHANT))) (MEM (V1 (:VAR (T)) (:VAL (CLYDE))))))

(AVB (V1 (:VAR (T)) (:VAL (CLYDE))))

(GREY)

(M2 (IS (GREY))) (COLOROF (V1 (:VAR (T)) (:VAL (CLYDE))))

(ELEPHANT)

(M1 (CLASS (ELEPHANT))) (MEM (V1 (:VAR (T)) (:VAL (CLYDE))))

(V1 (:VAR (T)) (:VAL (CLYDE))))

(X (:VAL (V3 (:VAR (T)) (:VAL (CLYDE))))

(DUMPED)

386 MSECS

$* (LISP)

END SNEPS

$? (EXIT)

END ALISP RUN
References

Bi-directional Inference. Technical Report No. 174,
Department of Computer Science, SUNY at Buffalo, Amherst,
NY, 32pp.