Sept 22, 2017

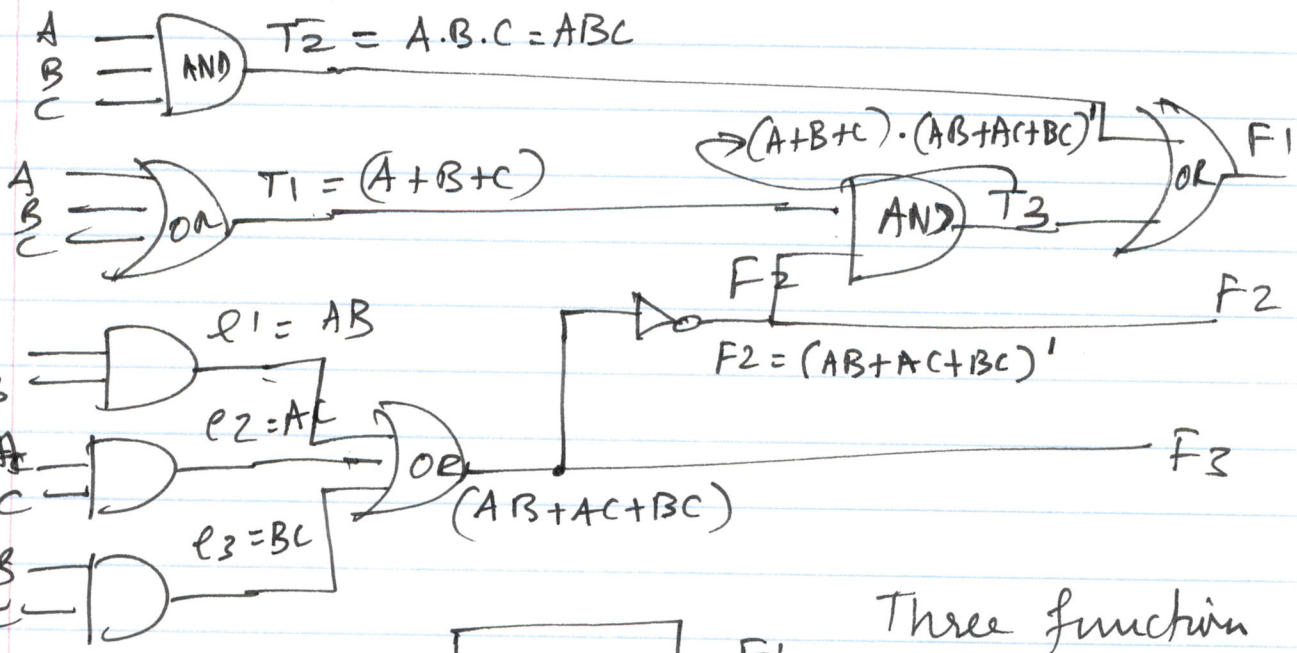
Problem

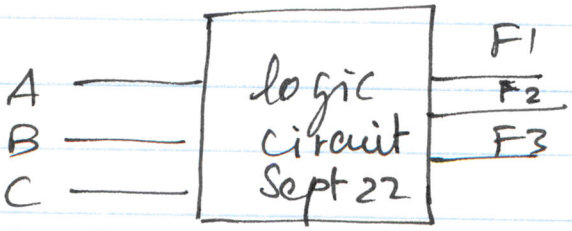
code

Circuit

Analysis → Reverse Engineering

Synthesis → Design & Implementation





Three functions
three outputs
4 inputs

$F1(A,B,C) = (\bar{A}+B+C)(AB+AC+BC)') + ABC$ — $F1(A,B,C) = ?$

$F2(A,B,C) = \overline{AB+AC+BC}$ — $F2(A,B,C) = ?$

$F3(A,B,C) = AB+AC+BC$ — $F3(A,B,C) = ?$

independent variables A, B, C

dependent variables F1, F2, F3

Scale of integration

Sept 22, 2017

integrated chips (circuit) — IC chips

Small scale integration
- SSI
- ≤ 1–10 gates
- E.g. 74LS00
- 4 NAND gates

Medium scale integration
- MSI
- MSI circuits
- ↓
- 10 ~ 100 gates
- e.g. 4-bit adder
- 3x8 decoder
- 4x1 Multiplexer

LSI
- large scale integration
- 100 ~ 1000 gates
- e.g. ALU
- Arithmetic Logic Unit

VLSI – CPU : VVLSI.

WSI – GPU

:

↓

multicore 4-core

↓

Tensorflow Processor

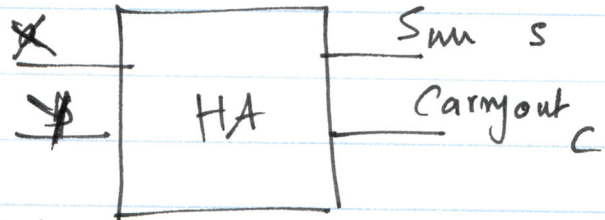
Half-adder. Design & implementation of a half-adder

2 HA – 1 FA

many n FA — n-bit adder

Sept 22, 2017

Half-adder



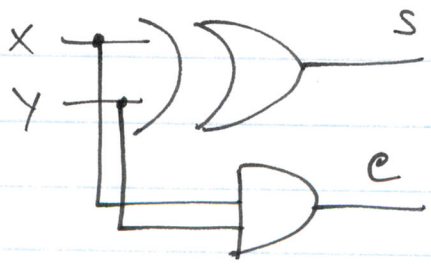
Truth Table: enumerate the operation

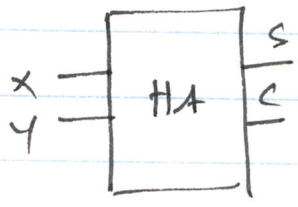
inputs		output	
x	y	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

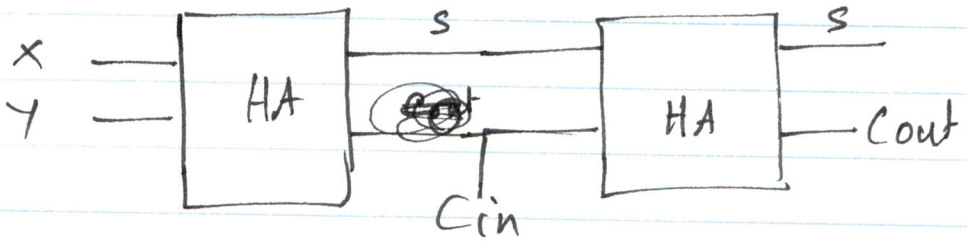
HA 2 bit binary addition.

$s(x,y) = x'y + xy'$ (XOR)

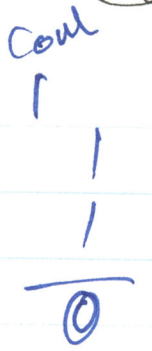
$c(x,y) = x \cdot y$ (AND)







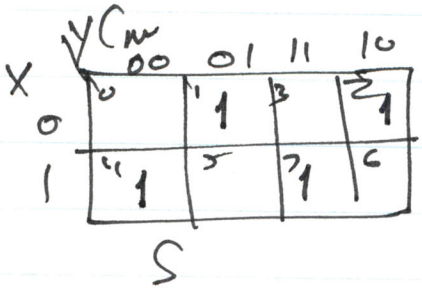
x	y	C_{in}	s	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

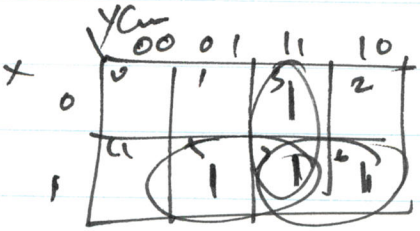


K-map

$S(x, y, C_{in}) = \Sigma(1, 2, 4, 7)$

$C(x, y, C_{in}) = \Sigma(3, 5, 6, 7)$





$C_{out} = yC_{in} + xC_{in} + xy$

$= \underline{\text{sof minterms}}$

~~SE~~ $S = x'y'C_{in} + x'yC_{in}' + xy'C_{in}' + xyC_{in}$

~~#KD~~ "Rewx"

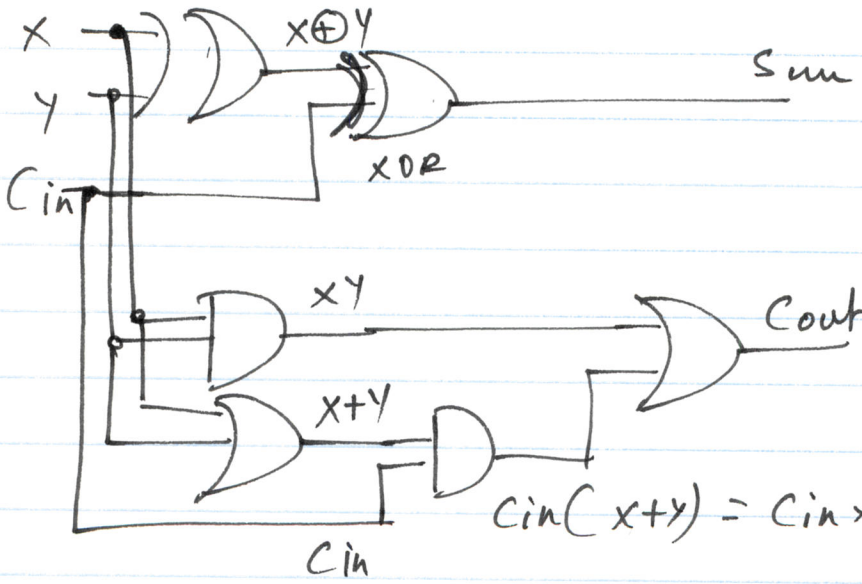
$= C_{in}'(x'y + xy') + C_{in}(x'y' + xy)$

$= C_{in}'(x \oplus y) + C_{in}(x \oplus y)'$

$= C_{in} \oplus x \oplus y$

$Cout = \cancel{Y_{Cin}} \; Y Cin + X Cin + XY$

$S = Cin \oplus X \oplus Y$



$Cin(X+Y) = Cin\,X + Cin\,Y$ ~~or~~

4-bit ↓ 8 bit adder

$4 \times 6 = 24$ gates

4-bit FA.